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Simulation and Experimental Research on a Schottky Gate Resonant Tunneling Transistor*

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Abstract: A Schottky gate resonant tunneling transistor (SGRTT) is fabricated. Relying on simulation by ATLAS software, we find that the gate voltages can be used to control the current of SGRTT when the emitter terminal is grounded and a positive bias voltage is applied to the collector terminal. When the collector terminal is grounded, the gate voltages can control the peak voltage. As revealed by measurement results, the reason is that the gate voltages and the electric field distribution on emitter and collector terminal change the distribution of the depletion region.

Key words: Schottky gate resonant tunneling transistor; device simulation; depletion region
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1 Introduction

In recent years, resonant tunneling transistors (RTTs) have attracted attention because they are among the fastest electronic devices in integrated circuit applications. Compared to conventional devices, RTTs have higher speeds of operation due to the short characteristic time of the tunneling process, lower power dissipation, and higher functionality[1,2]. Thus, RTTs are suitable for memory and logic circuits and research on RTT devices is of great importance.

RTT can be divided into gate RTTs and combination RTTs, which are an integration of RTD and HFET. The gate RTT consists of a Schottky gate structure and a p-n junction gate structure. This paper focuses primarily on the Schottky gate RTT (SGRTT). The material design, structure, and measurement are shown in the paper. As measured, we find new *I-V* characteristics. This behavior is simulated by the Silvaco software to reveal the physics mechanisms. It will be helpful to improve the techniques and to make good use of it for the future.

2 Material and device structure

Figure 1 shows the material layers of the SGRTT. The epitaxial layer was grown by molecular beam epitaxy on a semi-insulating GaAs substrate. The material layers are similar to the conventional RTD. The double-barrier structure consists of two 1.7nm-thick undoped AlAs barriers separated by a 5nm-thick undoped $In_{0.17}Ga_{0.83}As$ quantum well. Two 5nm-thick $In_{0.17}Ga_{0.83}As$ sub-wells are designed beside two barrier layers to improve the PVCR (peak to valley current ratio) parameter. The low-doped n^--GaAs emitter layer is introduced to enhance controllable capability of the device current by the gate voltage.

500nm	n^+-GaAs	$2\times10^{19}cm^{-3}$	top contact
50nm	n^--GaAs	$2\times10^{17}cm^{-3}$	emitter
100nm	n^--GaAs	$5\times10^{16}cm^{-3}$	
5nm	i-GaAs	undoped	spacer
5nm	i-$In_{0.17}Ga_{0.83}As$	undoped	sub-well
0.5nm	i-GaAs	undoped	spacer
1.7nm	i-AlAs	undoped	barrier
5nm	i-$In_{0.17}Ga_{0.83}As$	undoped	well
1.7nm	i-AlAs	undoped	barrier
0.5nm	i-GaAs	undoped	spacer
5nm	i-$In_{0.17}Ga_{0.83}As$	undoped	sub-well
5nm	i-GaAs	undoped	spacer
100nm	n^--GaAs	$5\times10^{16}cm^{-3}$	collector
50nm	n^--GaAs	$2\times10^{17}cm^{-3}$	
500nm	n^+-GaAs	$2\times10^{19}cm^{-3}$	bottom contact
SI GaAs substrate(100)			

Fig.1　Material structure of SGRTT

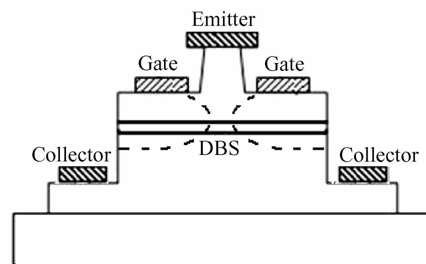

Fig.2　Schematic cross section structure of SGRTT (Solid lines correspond to the edge of depletion region)

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Figure 2 shows the schematic cross section structure. It contains three electrodes: Emitter (Au/Ge/Ni), gate (Ti/Pt/Au), and collector (Au/Ge/Ni). The emitter metal (Au/Ge/Ni) is evaporated first as a refuge of the etching gate mesa process later; the gate mesa and collector mesa are etched by the wet chemical etching process. The gate metallization is performed using the self-aligned evaporation and lift-off process. Where the schottky gate metal is in contact with the semiconductor, the depletion region exists under the gate and can be controlled by the gate voltage. The effective area of the mesa and, therefore, the current can be controlled efficiently by the gate voltage, particularly at the low-doped n^--GaAs emitter layer. For better current controlling capability of gate voltage, a 5μm × 5μm emitter area is chosen in this paper. The two gate electrodes can be closer because the length of the emitter is designed short enough. Thus, the depletion region under the gate electrode has more influence on the resonant tunneling current and a better transconductance parameter can be achieved[3].

3 Simulation of device

Based on the material layers and device structure in section 2, we adopt ATLAS software by Silvaco Inc. to simulate the structural and electrical properties. *I-V* characteristics and physical structure of SGRTT device can be achieved.

3.1 Result of simulation

Figure 3 shows the *I-V* characteristic of SGRTT. In Fig. 3 (a), the emitter (the top of device) is grounded and a positive bias voltage is applied to the collector (the bottom of device). In Fig. 3 (b), the collector is grounded and a positive bias voltage is applied to the emitter. Comparing the two simulation results, we find that when the top is grounded, I_P (peak current) and I_V (valley current) decrease with higher absolute value of gate voltages, but V_P (peak voltage) and V_V (valley voltage) are independent of it. Thus, the gate voltages can be used to control the current of SGRTT. When the bottom is grounded, V_P and V_V can be influenced by the gate voltage more obviously and I_P and I_V change slightly, so that the gate voltages can be used to control V_P.

3.2 Analysis

Based on the theory of semiconductor physics, the depletion region width is:

$$x_d = \left\{ - \frac{2\varepsilon\varepsilon_0 [(V_s)_0 + V]}{qN_D} \right\}^{1/2} \quad (1)$$

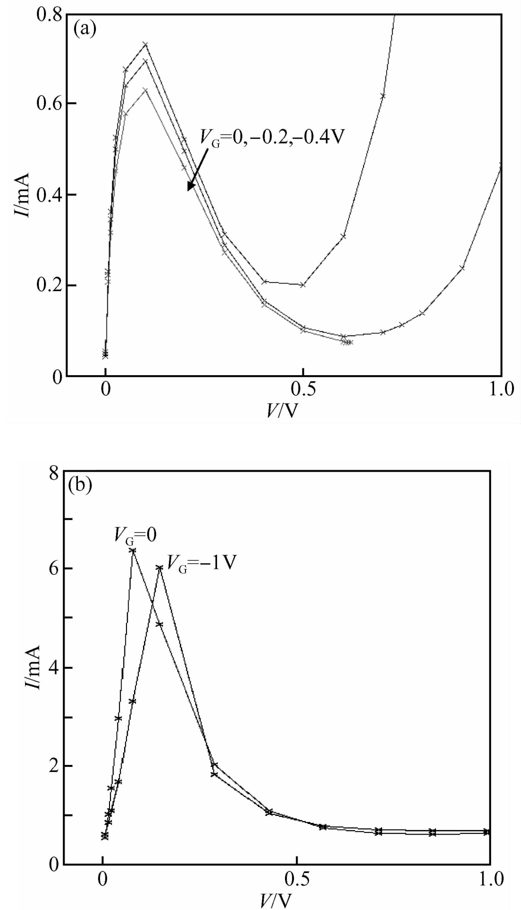


Fig. 3 Calculated *I-V* Characteristics of SGRTT (a) Emitter grounded; (b) Collector grounded

where V_s is the energy of the surface states of a vacuum, N_D is the doping concentration, V is the gate voltage, ε_0 is the permittivity of a vacuum, ε is the permittivity of GaAs, and q is the electronic charge. When the emitter is grounded, the position of the depletion region is primarily under the gate metal. According to Eq. (1), the width of the depletion region becomes larger when the absolute value of the gate bias voltage increases; the horizontal expanse of depletion can squeeze the channel of collector-emitter current as a result of reducing the current. Figure 4 (a) shows the cross section of SGRTT in this situation. Thus, the gate voltages can be used to control the current of SGRTT.

In another case, the collector is grounded and a positive bias voltage is applied to the emitter. Because the emitter is in the high potential, the electric field concentrates to the mesa of SGRTT. Then the depletion region expends horizontally and perpendicularly, and unites as a whole at the end. In this situation, the position of the depletion region is in the upper position of the current channel, which is equivalent to a big resistance R blocking in the current channel, as shown in Fig. 4(b). The increment of voltage ΔV is:

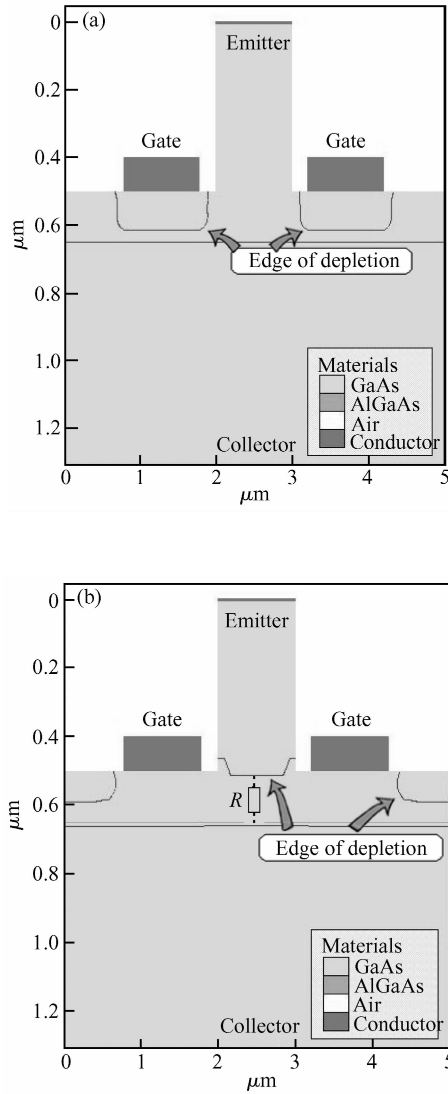


Fig. 4 Cross section structure of SGRTT's by calculation (a) Emitter grounded; (b) Collector grounded

$$\Delta V = RI \tag{2}$$

where I is the current from the emitter to collector.

Assuming the peak voltage is V'_{P}, when the collector is grounded and the gate is applied on a negative voltage,

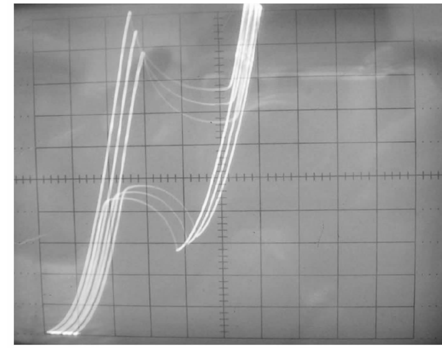
$$V'_{P} = V_{P} + \Delta V \tag{3}$$

where V_{P} is the peak voltage when the gate is grounded, thus $V'_{P} > V_{P}$.

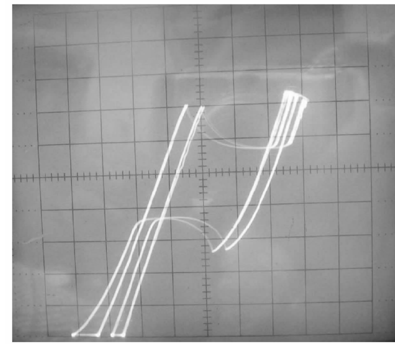
While applying higher gate voltage, R becomes larger and V'_{P} grows larger. As a result, the gate voltage can make the V_{P} move right towards the voltage axis without an obvious change of I_{P}. Therefore, when the collector is grounded, gate voltages can be used to control the peak voltage of the SGRTT device.

4 Experimental results

SGRTT devices are fabricated in two batches.



(a)



(b)

Fig. 5 Measured I-V Characteristics of SGRTT (a) x: 0.2V/div, y: 2mA/div, gate voltage step: −1V, emitter grounded; (b) x: 0.2V/div, y: 5mA/div, gate voltage step: −1V, collector grounded

The measurement is carried on at room temperature. The I-V characteristics when the emitter is grounded and the collector is grounded are both shown in Fig. 5. The I_{P}, I_{V}, PVCR, and other data extracted from Fig. 5 are illustrated in Tables 1 and 2.

The measurement results are similar to the simulation results: gate voltages can be used to control the I_{P} and I_{V} of SGRTT device when the emitter is grounded and to control the V_{P} and V_{V} when the collector is grounded. Although the layout and material layer design of the device are based on a completely symmetric structure, the characteristic of the I-V

Table 1 Parameters extracted from Fig. 5 (a) when emitter is grounded

	I_P /mA	I_V /mA	V_P /V	V_V /V	PVCR	PVVR	$(\Delta I_P/\Delta V_G)$ /mS	$\Delta V_P/\Delta V_G$
$V_b = 0V$	20.2	5.	0.52	0.75	3.67	0.69		
$V_b = -1V$	19.1	6.0	0.55	0.81	3.18	0.68	1.1	0.03
$V_b = -2V$	17.7	6.5	0.60	0.87	2.72	0.69	1.4	0.05

Table 2 Parameters extracted from Fig. 5 (b) when collector is grounded

	I_P /mA	I_V /mA	V_P /V	V_V /V	PVCR	PVVR	$(\Delta I_P/\Delta V_G)$ /mS	$\Delta V_P/\Delta V_G$
$V_b = 0V$	35.5	13.1	0.92	1.04	2.71	0.88		
$V_b = -1V$	35	13.4	1.02	1.12	2.61	0.91	0.5	0.3

curve shows asymmetric behavior. We discussed the main reason for this in section 3.

This finding is important for applications of digital circuits. Taking the logic circuit as an example, the state of the MOBILE[4,5] (monostable-bistable transition logic element) circuit is determined by the magnitude of I_P of the drive RTT which can be controlled by the gate voltages. However, the operation of the digital switch[6] is determined by the value of V_P. Therefore, the asymmetric *I-V* characteristics of SGRTTs can influence the application in the digital circuit.

5 Conclusion

Schottky Gate RTTs are fabricated and measured. Through simulation by ATLAS software, we find that gate voltages can be used to control the current of SGRTT when the emitter is grounded and to control the V_P when the collector is grounded. The measurement results prove this asymmetric behavior in *I-V* characteristics. According to the theory of the depletion region, this paper reveals the physical mechanisms. It is also shown that this behavior can greatly influence the application in the digital circuit.

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基于肖特基栅共振隧穿三极管的器件模拟与实验分析*

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摘要： 通过流片，制作出肖特基栅共振隧穿三极管(SGRTT).根据ATLAS软件的模拟发现，当发射极接地，集电极接外加偏压时，栅极电压对于SGRTT的电流起到明显的控制作用.当集电极接地，栅极电压会主要影响峰值电压，其原因是栅极电压和发射极、集电极的电场分布将会改变耗尽区的分布.实验测试结果对这种现象也予以证实.

关键词： 肖特基栅共振隧穿三极管；器件模拟；耗尽区

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