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The Bipolar Field-Effect Transistor: III. Short Channel Electrochemical Current Theory (Two-MOS-Gates on Pure-Base)*

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Abstract: This paper describes the short channel theory of the bipolar field-effect transistor (BiFET) by partitioning the transistor into two sections, the source and drain sections, each can operate as the electron or hole emitter or collector under specific combinations of applied terminal voltages. Analytical solution is obtained in the source and drain sections by separating the two-dimensional trap-free Shockley Equations into two one-dimensional equations parametrically coupled via the surface-electric-potential and by using electron current continuity and hole current continuity at the boundary between the emitter and collector sections. Total and electron-hole-channel components of the output and transfer currents and conductances, and the electrical lengths of the two sections are computed and presented in graphs as a function of the D.C. terminal voltages for the model transistor with two identical and connected metal-oxide-silicon-gates (MOS-gates) on a thin pure-silicon base over practical ranges of thicknesses of the silicon base and gate oxide. Deviations of the long physical channel currents and conductances from those of the short electrical channels are reported.

Key words: bipolar field-effect transistor theory; MOS field-effect transistor; simultaneous electron and hole surface and volume channels; surface potential; short channel theory; double-gate pure-base

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1 Introduction

The silicon MOS field-effect transistor (FET) technology is advancing into the nanometer dimensions in the form of double-gate and thin pure-base, fin-like structure, known as the FinFETs[1]. Their experimental electrical current-voltage characteristics, recently reported by IMEC with Assignees from four companies[2], could not be accounted for[3] by the traditional 55-year-old unipolar field-effect theory of the p/n junction-gate field-effect transistor (JGFET) invented and theorized by Shockley in 1952[4,5], and reduced to practice by Dacey and Ross[6]. This 1952-Shockley theory was followed by recent device theorists and engineers to compact model the MOS-gate and Insulator-Gate FETs (MOSFET and IGFET) single-gate semi-infinite-thick-base "bulk" transistors[7,8] and also the FinFETs which was extensively and carefully reviewed by Ortiz-Conde-Garcia-Sanchez-Liou in January 2007[9]. It was soon theorized and demonstrated (in March 2007)[3] and later presented by us[3,10~13] that the observed experimental current-voltage characteristics reported by IMEC + Assignees[2] showed distinct bipolar behavior, namely the simultaneous presence of both electron and hole surface-inversion-channel currents, even a hint of volume-channel currents, giving six channels in their two-MOS-gates on thin-base FinFET structures. The IMEC data covered wide ranges of oxide and base thicknesses and gate or base lengths, and also drain-source contact types, giving confidence that the random variations observed in these first-silicon transistors fabricated by the initial-nanometer-technology do not mask the observed bipolar nature in the current voltage characteristics in these FinFETs. After several iterations of alternatives, we named our discovery of the bipolar nature of the FET and our theory, the 100% <u>Bipolar Field Effect Transistor</u> (BiFET) Theory[3,10~13], to replace and to complete the now 55-year-old Shockley's 1952 <u>Unipolar Field-Effect Transistor Theory</u> (UniFET) which is a 25% FET theory that considered only one current, the drift of one carrier species[4~6,14,15], while our present new BiFET theory contains all four currents, drift and diffusion of both

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electron and hole carrier species[3,10~13]. This 100% BiFET theory also replaces the 1966 Sah-Pao theory[15,16] for the 'bulk' MOSFET which included both the drift and the diffusion currents, again for only one carrier species, the electron or the hole, but not both, thus, the 50% BiFET or the UniFET theory. Such a BiFET property, in one transistor structure, was conceived as early as 1970 by one of us (possibly by others in even earlier reports in the thin film transistor literature, which we have not found in the digital database thus far) in the form of a complementary pair of FETs in the simple bulk inversion MOSFET structure with a p/n junction isolated n-type basewell, which was soon experimentally demonstrated and reported in 1971-Fu-Sah[17], showing bistable negative conductance *I-V* characteristics in a FET containing a surface-inversion-channel pMOST in the n-basewell on a p-Si substrate-body, and a n-volume-channel nJGFET (n-basewell/p-substrate Junction-Gate FET). The unique feature 'designed' by Sah in this 1971-Fu-Sah BiFET was the four contacts to the n-basewell, consisting of a p^+ and a n^+ source and also drain contacts to the n-basewell. The traditional two contacts to the UniFET n-basewell of the pMOST are the one p^+ drain and one p^+ source rectifying contact to the inversion p-type surface-channel on the n-type basewell. These two unique and novel n^+ high/n-low non-rectifying n^+ drain and n^+ source junctions severed as the low-resistance contacts to the n-basewell or the n-type volume-channel of the nJGFET. The bistable negative conductance *I-V* characteristic was obtained by proper interconnection of the four basewell contacts with gold wires as illustrated in 1971-Fu-Sah[17].

One of the most important FET features, not recognized and discussed since the 1952-Shockley invention of the Field Effect Transistor[4], the 1953-Prim-Shockley detailed two-section device analysis[5] and the 1953-Dacey-Ross reduction to practice[6], is the concept of Debye length. The Debye length is the decay length of the 3-dimensional spatial redistribution of mobile ion density (or concentration) to 'screen' a fixed (immobile) charge or charge distribution, a concept which was and is well known in electrochemistry. This was imported into the many-body (body = ion = electron) solid-state theory, which is carried to the first order by the theorists via linearization (small-signal model in electrical engineering) of the Boltzmann (dilute) or Fermi (dense) distribution of the mobile ions or electrons as a function of the macroscopic electric potential in accordance to the Coulomb force law between two point charges. The Debye length concept was introduced into semiconductor device physics by Shockley in the 1949-Shockley invention of the Bipolar Junction Transistor (BJT)[18] to demonstrate quantitatively the incompleteness or effectiveness of screening of microscopic or electron and hole and nuclear or ionic-core point-charges, macroscopic or many point-charges, and charge distributions in a semiconductor device structures, by the mobile electrons and holes, such as an abrupt change of the impurity ion concentrations in a p/n junction, and also in a much gradual spatial variation of the impurity ion concentration in an impurity-ion diffused or/and implanted semiconductor region. Shockley mathematically showed[18] that regional or local charge neutrality is established by the presence of a high concentration of electrons and holes which screen the fixed charges and charge distributions. His linearly graded p/n junction example showed quantitatively that local 'uncompensated' or 'not-neutralized' space charges or space charge distributions will appear when electrons and holes are depleted by a local electric field to have very low concentrations or the gradient of the ion concentration is high in a graded p/n junction. This electrical screening from Coulomb force has been represented in the quantum-statistical-mechanics many-body theory (many electrons and holes) by the linearized (small fluctuation or small signal approximation) local Debye Length $L_D = \{\varepsilon_{Si} kT/[q^2(N+P)]\}^{1/2}$. In metals, this is an extremely small length due to the very high concentration of mobile electrons, $N \approx 5 \times 10^{22}\,cm^{-3}$ making screening highly effective. In pure silicon, the mobile electron and hole concentration is a meager $N = P = n_i = 10^{10}\,cm^{-3}$ at room temperature, giving a Debye length $25\mu m$ to $30\mu m$ and hence, rather ineffective local screening of charged small objects. This carrier screening length in pure semiconducting silicon is one thousand times larger than the dimensions of the nanometer transistors in pure silicon, such as the double-gate on pure base MOS FinFET, experimentally fabricated[2], qualitatively and quantitatively analyzed[3,10,11] and recently analyzed in details[12,13]. Even in the impure-base of the inversion surface-channel of a 'bulk' MOSFET, such as an nMOST with p-base of $P = P_{IM} = 1.0 \times 10^{16}\,cm^{-3} \gg N = n_i^2/P = 10^{20}/10^{16} = 10^4\,cm^{-3}$, the Debye screening length is still quite large, $L_D = (25 \sim 30\mu m) \times (10^{16}/2 \times 10^{10})^{-1/2} = 35nm$ to $70nm$. This is still comparable with, not much smaller than, the physical dimensions of the present and future nanometer MOSFETs. Thus, space-charge neutrality is untenable, although it is certainly still a good first step in compact-model simulation of FETs and other semiconductor devices, such as the often used assumption of quasi-neutrality in the

base of the BJT[18] and of carrier depletion in the surface space-charge layers of MOST and MOSC (Transistors and Capacitance)[7,8].

A second factor on analyzing a realistic FET, that takes into account of its generic short-channel nature we just described, is the fact that FET is inherently a two-dimensional device because of its operation principle, first succinctly stated by Lilienfeld in his 1930 patents, namely, longitudinal conductivity modulation by a transverse electric field which induces and controls the density of the charge-carrying mobile particles or carriers, the electrons[19]. (Concept of holes was not developed until a few years later by Wilson applying quantum mechanics to describe semiconductors.) It is two dimensional if it is uniform in the width direction of the semiconductor sheet, to be scaled along the z-axis, which we shall assume in this report, otherwise the nanometer FET would be three-dimensional. In order to serve as the device-physics benchmark for developing compact models, we need to obtain an accurate analytical solution to circumvent the numerical accuracy limitation of two-dimensional numerical analysis such as the finite element method. For this purpose, the two-dimensional short and thin transistor is partitioned into several sections (The simplest or zeroth order model, is the two section model used in this report.) and each section is solved by two one-dimensional equations, one each in the x and y directions, which are coupled parametrically by the surface potential, first devised by Sah in 1966-Sah-Pao[15,16] to analyze the MOS transistor diffusion current in addition to drift current. Those few historical investigators, who obtained the diffusionless drift-current unipolar solutions for thin-film and SOI (semiconductor on insulator) FETs with insulated gate(s), did indeed follow the two-section gradual-channel method introduced in the 1952-Shockley invention of the Junction-Gate FET[4~6], in which the transistor is partitioned into two sections along its length from the source to the drain in parallel to the single gate or two parallel gates. We shall label these two sections as the source emitter section and drain collector section. This 2-section physical or geometrical partitioning has also been used in FETs with the MOS gate(s), namely, the MOSFETs. The presumed justification of using the Shockley 2-secton model is that the electric field in the surface channel(s) of the source emitter section is dominantly transverse to the current flow, while the electric field in the drain collector section, if it exists from proper biasing, is predominantly parallel to the current flowing in the drain volume-channel. Such a drain collector section does appear after the FET is biased into the surface-channel current saturation range. This is in the voltage range when the drain/source voltage is larger than the gate/source voltage. In our discussion and analyses, all the contact potential differences or threshold voltages at the three contacts of the three terminals, S, G, and D, are absorbed into the voltage applied between the terminals and a universal reference terminal of potential node point. In addition to the drain section serving as the collector of the first carrier species (say electrons for $0 < V_{GS} > = < V_{DS}$), the surface channel for the second carrier species (holes) also appear because the Gate/Drain applied voltage is larger than the threshold voltage to induce a surface inversion channel(s) of the second carrier species (hole) starting at the drain or $y = L$. So the same equations for the first carrier species (such as electrons for $0 < V_{GS} > = < V_{DS}$) are trivially extended the unipolar FET theory to cover the bipolar conduction simultaneously by two carrier species (electrons and holes) at higher drain voltages. In this third report of the proposed 5-report (just increased to 6-report) series on BiFET, we shall provide the analytical solutions in the two-sections of the transistor in order to take into account of the short-channel effect. Families of graphs are computed and given, which are (I_D-V_{GS}), (I_D-V_{DS}), (g_{ms}-V_{GS}), (g_{ms}-V_{DS}), (g_{ds}-V_{GS}) and (g_{ds}-V_{DS}) and also the channel section length, y_0-V_{GS} and y_0-V_{DS}. Their deviations from the one-section long-channel solution[12], useful for compact modeling, is also described in this report.

2 Short Channel Theory of the Two-Gate on Pure-Base Transistors

The voltage and current equations of the UniFET theory with single-gate on thick or semi-infinite impure-base from Electrochemical Potential Theory given in 1966-Sah-Pao[14~16] and from the Drift-Diffusion Theory given in 1996-Sah[20~22] were modified for the BiFET with two identical gates on a thin pure-base[3,10~13]. They are immediately applicable to each of the two sections separated by the boundary $y = y_0(x)$ with the additional equations from matching the potential and current density solutions in the two sections at the boundary. We shall use our 40+year notation and coordinate system from[3,7,10~16,20~22] summarized as follows. The variables are functions of the 2-dimensional coordinates (x, y) with no variation along the width of the gate and channel in the z-direction from $z = 0$ to $z = Z = W$. The y-axis is the direction of the channels and the x-axis, the SiO_2/Si interfacial planes of the two gates, located at $x = 0$ and $x = x_B$ with base thickness x_B. The two gate oxides have

equal electrical thickness of x_O. The impurity concentration in the pure base is zero, $P_{IM}=0$, and for impure base of spatially constant concentration, $P_{IM}(x,y)=P_{IM}\neq$ function of (x,y). The concentrations of the traps or generation-recombination-trapping centers are assumed zero in both the base region and at the two gate-oxide/pure-base interfaces. The source and drain contacts to the pure-base are located respectively at $y=0$ and $y=L$. The effects from the contacts will be described in a later report. The three potential variables are normalized to kT/q and denoted by $U_\alpha = qV_\alpha/kT$ where respectively, $\alpha=N,P$, and I are for the electron and hole electrochemical, and the electric potentials and I for midgap or intrinsic is usually omitted. Near thermal equilibrium (low electric field or no hot carriers) is assumed, so the Einstein relationship between mobility and diffusivity holds for electrons and holes, $D_n/\mu_n=(kT/q)$ and $D_p/\mu_p=(kT/q)$ where $T=T_L$ is the lattice or heat-transfer temperature. The Poisson Equation and the electron and hole current equations are then given by the classical macroscopic equations which are three non-zero-trapping equations of the six Shockley Equations of electric charge transport in solids[7]. The terminal currents are denoted by I_T. T = D (drain), S (source), G1 (gate-1), G2 (gate-2), B (Base).

$$\nabla\cdot(\varepsilon_S\boldsymbol{E})=\rho(x,y,z)=q(P-N-P_{IM}) \quad \text{3-Dimensional Impure} \quad (1)$$

$$=\varepsilon_S[(\partial E_X/\partial x)+(\partial E_Y/\partial y)]=q(P-N-P_{IM}) \quad \text{2-Dimensional Impure} \quad (2)$$

$$=\varepsilon_S[(\partial E_X/\partial x)+(\partial E_Y/\partial y)]=q(P-N) \quad \text{2-Dimensional Pure} \quad (3)$$

$$=qn_i[\exp(U_P-U)-\exp(U-U_N)] \quad (3A)$$

Electrochemical Current Theory

$$I_{DN}=-(W/y_0)\iint[qD_nN(\partial U_N/\partial y)]\partial x\partial y \quad (x=0 \text{ to } x_B;\ y=0 \text{ to } y_0) \quad (4)$$

$$I_{DP}=-[W/(L-y_0)]\iint[qD_pP(\partial U_P/\partial y)]\partial x\partial y \quad (x=0 \text{ to } x_B;\ y=y_0 \text{ to } L) \quad (5)$$

Drift and Diffusion Current Theory

$$I_{DN}=-(W/y_0)\iint[q\mu_nNE_Y+qD_n(\partial N/\partial y)]\partial x\partial y \quad (x=0 \text{ to } x_B;\ y=0 \text{ to } y_0) \quad (6)$$

$$I_{DP}=-[W/(L-y_0)]\iint[q\mu_pPE_Y+qD_p(\partial P/\partial y)]\partial x\partial y \quad (x=0 \text{ to } x_B;\ y=y_0 \text{ to } L) \quad (7)$$

$$I_D=I_{DN}+I_{DP}=-I_S \quad (8)$$

Using $E_X=(kT/q)(\partial U/\partial x)$ and $E_Y=(kT/q)(\partial U/\partial y)$, and the x-independent electrochemical potential assumption[3,7,10~16,20~22], expressed by $U_P(x,y)=U_P(y)$ and $U_N(x,y)=U_N(y)$, we get the 1-dimensional (1-D) Gauss Law from converting the volume integration of the Poisson Equation (1) ($\partial x\partial y\partial z=\mathrm{d}\mho$) into a surface integration using the divergence theorem $\oiiint\nabla\cdot(\varepsilon_O\boldsymbol{E})\mathrm{d}\mho=\oiint(\varepsilon_O\boldsymbol{E})\cdot\mathrm{d}\boldsymbol{S}$ with the line integrals $\int(\partial/\partial y)(\varepsilon_OE_Y)\partial x$ ($x=-x_O$ to 0 for MOS gate-1 and x_B to x_B+x_O for MOS gate-2) omitted as next order 2-Dimensional corrections:

$$\varepsilon_SE_X(x=0,y)=-C_O[V_{GB}-V_{FB}-V(x=0,y)] \quad (9)$$

$$\varepsilon_SE_X(x=x_B,y)=+C_O[V_{GB}-V_{FB}-V(x=x_B,y)] \quad (10)$$

Using $V(x=0,y)=V(x=x_B,y)=V_S(y)=U_S(y)(kT/q)$, $V(x=x_B/2,y)=U_0(y)(kT/q)$, and $E_X(x=0,y)=E_X(x=x_B,y)=E_S(y)$, and invoking the x-symmetry about the mid-plane of the base-layer $E_X(x=x_B/2,y)=0$ for two identical gates where $U(x=x_B/2,y)=U_0(y)$ is the minimum or maximum, then we have the following result from the Gauss Law in the one-dimensional approximation with the two-dimensional term omitted, which gave Eqs. (9) and (10)

$$U_{GB}-U_{FB}-U_S=U_{GB}-U_S=(\mathrm{sign}U_S)\times(C_D/C_O)\times F_0(U_S,U_P,U_N,U_0) \quad (11)$$

$$F_0(U,U_P,U_N,U_0)=\{[\exp(U-U_N)-\exp(U_0-U_N)]+[\exp(U_P-U)-\exp(U_P-U_0)]\}^{1/2} \quad (12)$$

$$x_B/(2L_D)\equiv X_B/2=\int(\mathrm{sign}U)[F_0(U,U_P,U_N,U_0)]^{-1/2}\partial_xU \quad (13)$$

where the x-integration is taken from $U=U_0$ to U_S. $L_D=(\varepsilon_skT/2q^2n_i)^{1/2}$ is the Debye screening length ~ 26μm at room temperature. U_{FB} is absorbed into the gate voltage U_{GB}. In the electron emitter section[3,10~13], the electron terms dominate and the hole terms can be neglected for the initial guess. In the hole emitter section[3,10~13], the hole terms dominate and the electron terms can be neglected for the initial guess. Thus, the initial guess solution of Eq. (13) in the electron emitter section is given by

$$x_B/L_D\equiv X_B=2\int(\mathrm{sign}U)\{\exp(U-U_N)-\exp(U_S-U_N)+(C_O/C_D)^2(U_{GB}-U_S)^2\}^{-1/2}\partial_xU \quad (14)$$

where the integration is from $U=U_0=U_N+\ln[\exp(U_S-U_N)-(C_O/C_D)^2(U_{GB}-U_S)^2]$ to U_S. This is the unipolar initial guess for the bipolar solution. The next order solution is reached by adding the omitted two terms from electrons or holes. These fourteen equations can be solved iteratively in the two physical sections, of electrical length of $y=0$ to y_0 for the electron source emitter section and hole source

collector section, and $y = y_0$ to L for the electron drain collector section and the hole drain emitter section. The most important, missed by everyone thus far, including us for a duration until November 30, 2007, was the correct source and drain terminal values of the two electrochemical potentials, $U_N(y=0) = U_{NS}$, $U_N(y=L) = U_{ND}$, $U_P(y=0) = U_{PS}$ and $U_P(y=L) = U_{PD}$, although the correct values were used to construct the 2-D distributions of $U(x,y)$, $U_N(y)$ and $U_P(y)$, the current density vectors, $\mathbf{J}_N(x,y)$ and $\mathbf{J}_P(x,y)$ and the carrier concentrations $N(x,y)$ and $P(x,y)$, seven months earlier for presentation at the Late News on May 23, 2007[3]. The correct ones are $U_{NS} = U_{SB}$ and $U_{PD} = U_{DB}$. In addition, at the flatband line, $y(x) = y_0$, $U(x = x_B/2,\ y = y_0) = U_0(y_0) = U_P(y_0) = U_N(y_0) = U(x = x_B, y = y_0) = U_S(y_0) = U_{GB}$ where $U_{FB} = 0$ or absorbed into the voltage applied to the gate. For two asymmetrical gates, the symmetrical solution just given can be extended to find the flatband line $y = y_0(x)$. The assumption of identical source and drain regions can also be extended. In this first characterization of the bipolar MOSFET, we have assumed that the drain and source regions of the thin pure base are identical, therefore, the use of the words "source" and "drain" to label these two ends of the thin pure-base is entirely arbitrary. Nevertheless, to connect this new bipolar FET to the past unipolar FET terminology coined by Shockley in 1952 and used by all subsequent engineers and scientists until today, we will name them[3,10~13] as the source electron emitter section which simultaneously is also the source hole collector section. Similarly, the drain electron collector section is simultaneously also the drain hole emitter section. This creates a semantic conflict of the words drain and emitter, and source and collector. Therefore, it may be preferable to discard the arbitrary designation of drain and source at the two ends of the base layer of the bipolar thin-base FET, and retain the bipolar junction transistor terminology of emitter and collector, which were also coined by Shockley, in 1949, for the bipolar junction transistor[18], noting the only difference between the two is that drift current dominates in the FET operation and diffusion current dominates in the BJT operation, regardless of the conductivity type of the base layer.

The electron emitter section and hole collector section occupy the same physical space of the bipolar field-effect transistor. This is a previously unrecognized cardinal feature of the BiFET or all FETs. The differential form of electrochemical current theory can be applied in the electron and hole collector channel sections:

$$I_{DN} = -qD_n W(\partial U_N/\partial y)\int N(x,y)\,\partial x \quad (x = 0 \text{ to } x_B;\ y = y_0 \text{ to } L) \tag{15}$$

$$I_{DP} = -qD_p W(\partial U_P/\partial y)\int P(x,y)\,\partial x \quad (x = 0 \text{ to } x_B;\ y = 0 \text{ to } y_0) \tag{16}$$

where the integrations $\int N(x,y)\,\partial x$ and $\int P(x,y)\partial x$ are carried out using the unipolar initial guess of the x-voltage-equations (11), (12) and (13) in the emitter regions. The following equations are derived from the unipolar initial guess of the current equations (4), (5), (15), (16):

$$I_{DN} \times y_0 = WD_n C_O(kT/q)\int 2(U_{GB} - U_S)\,\partial_y U_N \quad (U_N = U_{SB} \text{ to } U_{GB}) \tag{17}$$

$$I_{DP} \times (L - y_0) = WD_p C_O(kT/q)\int -2(U_{GB} - U_S)\partial_y U_P \quad (U_P = U_{GB} \text{ to } U_{DB}) \tag{18}$$

$$\int \exp(-U_N/2) \times [F_{Ch}(U_S,U_0)]^{-1}(C_O/C_D)2(U_{GB} - U_S)\partial_y U_N \quad (U_N = U_{SB} \text{ to } U_{GB}) = (I_{DN}/I_{DP})(D_p/D_n)[\exp(U_{GB}) - \exp(U_{PS})] \tag{19}$$

$$F_{Ch}(U_S,U_0) = \int \exp(-U) \times [\exp(U) - \exp(U_0)]^{-1/2}\partial_x U \quad (U = U_0 \text{ to } U_S \text{ in electron emitter}) \tag{20}$$

$$\int \exp(+U_P/2) \times [F_{Ce}(U_S,U_0)]^{-1}(C_O/C_D)(-2)(U_{GB} - U_S)\partial_y U_P \quad (U_P = U_{GB} \text{ to } U_{DB}) = (I_{DP}/I_{DN})(D_n/D_p)[\exp(-U_{GB}) - \exp(-U_{ND})] \tag{21}$$

$$F_{Ce}(U_S,U_0) = \int -\exp(U) \times [\exp(-U) - \exp(-U_0)]^{-1/2}\,\partial_x U \quad (U = U_0 \text{ to } U_S \text{ in hole emitter}) \tag{22}$$

From the above six equations, the following initial-guess solution of the ratio of the electron current to the hole current, I_{DN}/I_{DP}, and the flatband line y_0, are obtained and given below:

$$\text{FIN} \equiv WD_n C_O(kT/q)\int 2(U_{GB} - U_S)\partial_y U_N \quad (U_N = U_{SB} \text{ to } U_{GB})$$

$$\text{FIP} \equiv WD_p C_O(kT/q)\int -2(U_{GB} - U_S)\partial_y U_P \quad (U_P = U_{GB} \text{ to } U_{DB})$$

$$\text{FCN} \equiv \int \exp(-U_N/2) \times [F_{Ch}(U_S,U_0)]^{-1}(C_O/C_D) \times 2(U_{GB} - U_S)\partial_y U_N \quad (U_N = U_{SB} \text{ to } U_{GB})$$

$$\text{FCP} \equiv \int \exp(+U_P/2) \times [F_{Ce}(U_S,U_0)]^{-1}(C_O/C_D) \times (-2)(U_{GB} - U_S)\partial_y U_P \quad (U_P = U_{GB} \text{ to } U_{DB})$$

$$I_{DN}/I_{DP} = (D_n/D_p) \times [(\text{FCN}/\text{FCP})^{1/2} \times \exp(-U_{GB}) \times (\text{FIN}/\text{FIP})]^{1/2} \tag{23}$$

$$y_0/L = 1/[1 + (I_{DN}/I_{DP}) \times (\text{FIP}/\text{FIN})] \tag{24}$$

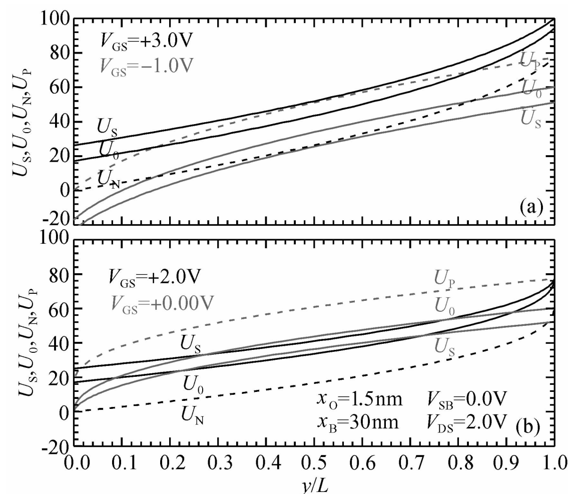

Fig. 1 Spatial variation along the channel length or y-direction of the surface potential U_S, the mid plane potential U_0, the electron quasi-Fermi potential U_N and the hole quasi-Fermi potential U_P. This is from the initial solution of the BiFET theory with the minority carriers excluded. The BiFET has the two identical MOS gates on a thin pure base. $x_O = 1.5$nm, $x_B = 30$nm, $V_{SB} = 0.0$V, $V_{DS} = 2.0$V. (a) $V_{GS} = -1.0$V and 3.0V; (b) $V_{GS} = 0.0$V and 2.0V. There is only the hole emitter ($y_0 = 0$) when $V_{GS} = -1.0$ and 0.0V or electron emitter ($y_0 = L$) when $V_{GS} = 2.0$ and 3.0V.

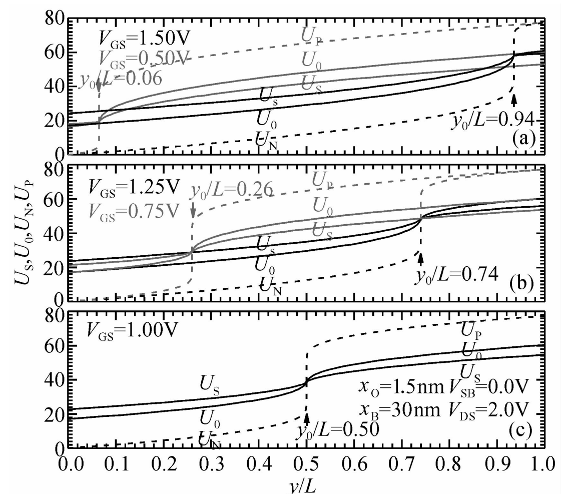

Fig. 2 Spatial variation along the channel length or y-direction of the surface potential U_S, the mid plane potential U_0, the electron quasi-Fermi potential U_N and the hole quasi-Fermi potential U_P. This is from the initial solution of the BiFET theory with the minority carriers excluded. The BiFET has the two identical MOS gates on a thin pure base. $x_O = 1.5$nm, $x_B = 30$nm, $V_{SB} = 0.0$V, $V_{DS} = 2.0$V. (a) $V_{GB} = 0.5$V and 1.5V; (b) $V_{GB} = 0.75$V and 1.25V; (c) $V_{GB} = 1.0$V. The flatband line y_0 which separates the hole emitter section and the electron emitter section is labeled in the three figures by (a) $y_0/L = 0.06$, 0.94; (b) 0.26, 0.74; and (c) 0.50.

3 Computed Spatial Variations of the Potentials

A crucial hint in helping to arrive at the correct analytical solution is to obtain the boundary conditions of the four internal potentials by using the device or electron and hole physics to sketch the variation along the channel length, y, of the four potentials which are the electron and hole electrochemical potentials, $U_N(y)$ and $U_P(y)$, and the electric potential at the two identical SiO_2/Si interfaces, $U(x=0,y) = U(x=x_B,y) = U_S(y)$, and at the mid-plane, $U(x = x_B/2, y) = U_0(y)$. The key for guessing the y-variations (and also x-variations) of these four potentials is to use the simple device physics or electrostatics governed by the Coulomb force Law between point charges and macroscopic Poisson's Equation, and the assumed exponential representation (or the classical limit of the quantum statistical distribution, i. e., the Boltzmann distribution) of the electron and hole concentrations, $N(x,y) = n_i \times \exp(U - U_N)$ and $P(x,y) = n_i \times \exp(U_P - U)$. This immediately leads to the correct guess of the y-variations of these four potentials, $U_N(y)$, $U_P(y)$, $U_S(y)$ and $U_0(y)$. With this guess to arrive at the correct boundary conditions at the terminals for these four potentials, which we presented in the Late News reports[3] their y-variations along the entire physical length of the base channel, $y = 0$ to $y = L$, that is partitioned into two sections, the source section from $y = 0$ to $y = y_0$ and the drain section from $y = y_0$ to $y = L$, then, the normalized section lengths, y_0/L and $(L - y_0)/L$, can be computed from the exact analytical equations we derived which were given in the previous section. For simplicity of physics, the flatband plane, $y = y_0$, is chosen as the boundary between the two sections which was mentally visualized long ago by Sah and illustrated by him as a teaching guide on MOS transistor physics[23]. These variations of the four potentials along the channel length, in both the source and drain sections, were computed for many combinations of voltages applied to the gate and the drain terminals, V_{GB} and V_{DB}, with the source terminal as the reference, $V_{SB} = 0$. The graphs of one selected set for each of the two channel current ranges, the non-saturation and the saturation ranges, are presented in this report. Figures 1(a) and 1(b) are for four combinations of applied gate and drain voltages in the linear or non-saturation channel current range. Figures 2(a), 2(b) and 2(c) are for five combinations of applied gate and drain voltages in the channel current saturation range. The darker curves are for one combination of voltages and the lighter curves are for the symmetrical combination of voltages. The presence of the two sections, which is the unique feature of the FET, is shown at one glance (A1G) in the three figures for the current saturation

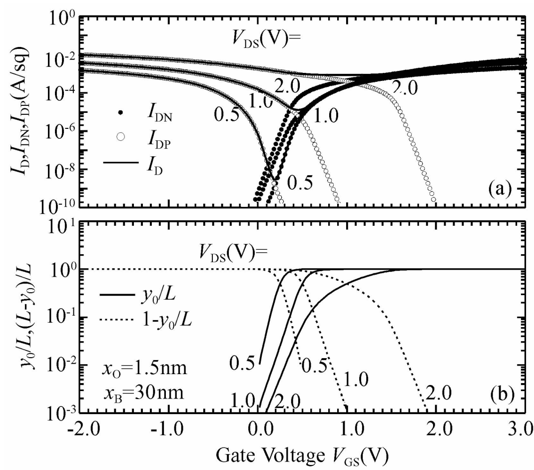

Fig. 3　Drain-source voltage V_{DS} dependence of the DC transfer current-voltage characteristics I_D-V_{GS}. The BiFET has two identical MOS gates on a thin pure base. x_O = 1.5nm, x_B = 30nm, V_{SB} = 0.0V. (a) The electron channel current I_{DN}, the hole channel current I_{DP} and the total drain current I_D. (b) The flatband line position y_0/L, the electron emitter section length y_0/L and the hole emitter section length $(L-y_0)/L$.

conditions given in Figs. 2(a), 2(b), and 2(c). The rapid change of the four potentials clearly delineates the boundary between the two sections, $y = y_0$. Higher order solutions are obtained by numerical iterations which are presented in a future report on the accuracy of the unipolar solutions in relation to the bipolar solutions and on the progression of the accuracy of the bipolar solutions with further iterations and with increasing impurity concentration in the base channel, important for compact modeling to design million-transistors circuits containing many signal-processing functions.

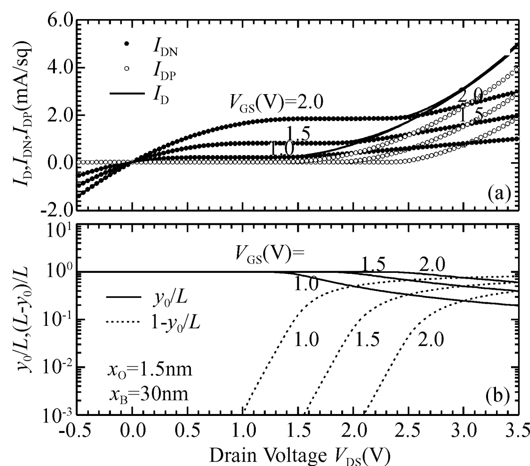

Fig. 4　Gate-voltage V_{GS} dependence of the DC output current-voltage characteristics I_D-V_{DS}. The BiFET has two identical MOS gates on a thin pure base. x_O = 1.5nm, x_B = 30nm, V_{SB} = 0.0V. (a) The electron channel current I_{DN}, the hole channel current I_{DP} and the total drain current I_D; (b) The flatband line position y_0/L, the electron emitter section length y_0/L, and the hole emitter section length $(L-y_0)/L$.

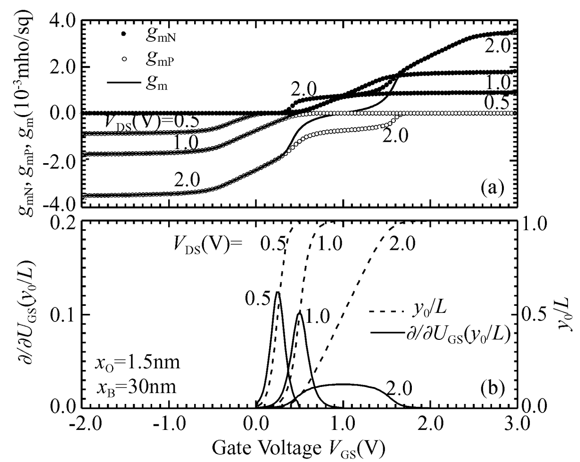

Fig. 5　Drain-source voltage V_{DS} dependence of the differential transconductance versus gate voltage characteristics. The BiFET has two identical MOS gates on a thin pure base. x_O = 1.5nm, x_B = 30nm, V_{SB} = 0.0V. (a) The total, and the electron and hole components of the transconductance. (b) The flatband line position y_0/L and its partial derivative with respect to gate voltage.

4　Computed Current-Voltage Characteristics and Channel Section Lengths

Selected results from computed terminal current-voltage and conductance-voltage characteristics are illustrated in twelve figures, Figs. 3 to 14. They take into account of the short electrical channel length, which is intrinsic to all FETs as explained in the preceding sections. Each of the first ten figures contains two parts, (a) and (b). The first parts, (a), are the current-voltage characteristics. The second parts, (b), are the voltage dependence of the electrical

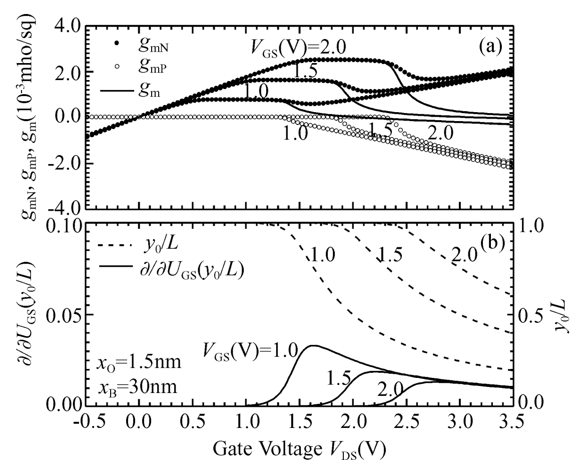

Fig. 6　Gate-voltage V_{GS} dependence of the differential transconductance versus drain voltage characteristics. The BiFET has two identical MOS gates on a thin pure base. x_O = 1.5nm, x_B = 30nm, V_{SB} = 0.0V. (a) The total, and the electron and hole components of the transconductance. (b) The flatband line position y_0/L and its partial derivative with respect to gate voltage.

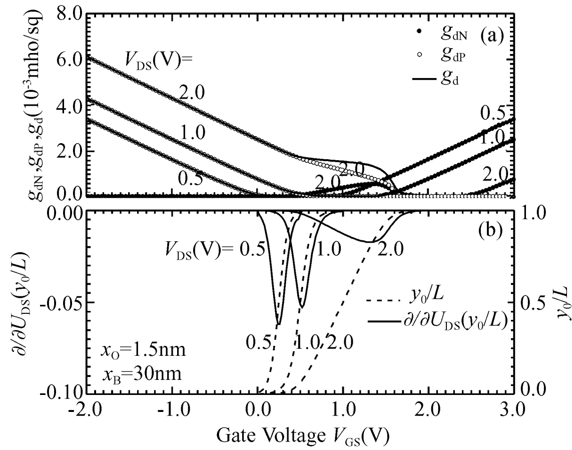

Fig. 7 Drain-source voltage V_{DS} dependence of the differential output conductance versus gate voltage characteristics. The BiFET has two identical MOS gates on a thin pure base. x_O = 1.5nm, x_B = 30nm, V_{SB} = 0.0V. (a) The total and the electron and hole components of the output conductance. (b) The flatband line position y_0/L and its partial derivative with respect to drain voltage.

channel length of the two sections, y_0 and $L - y_0$, in semilog scale in order to graphically show the small deviation of y_0 from L or 0, when the applied drain or gate voltage is near the drain current saturation value. For the conductance-voltage figures, Figs. 5～8, the second parts, (b), also contain the derivative of the section lengths with respect to the terminal voltage. We used the flatband line (2-D with no Z dependence) or surface (3-D with Z variation or flatband plane with no Z variation) as the electrical channel length, y_0, or boundary plane (y_0, z = 0 to W) that separates the two sections, the emitter and the collector sections.

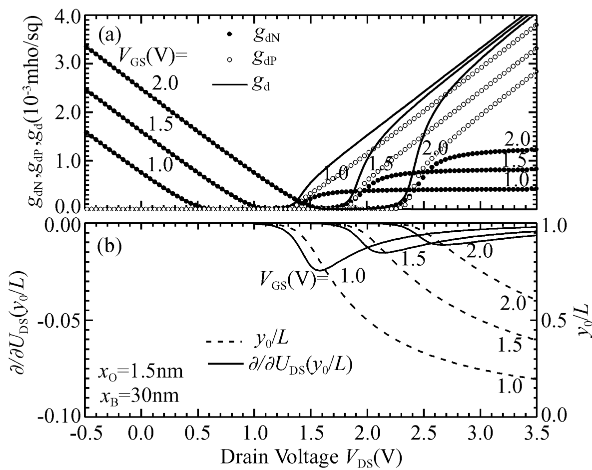

Fig. 8 Gate-voltage V_{GS} dependence of the differential output conductance versus drain voltage characteristics. The BiFET has two identical MOS gates on a thin pure base. x_O = 1.5nm, x_B = 30nm, V_{SB} = 0.0V. (a) The total and the electron and hole components of the transconductance. (b) The flatband line position y_0/L and its partial derivative with respect to drain voltage.

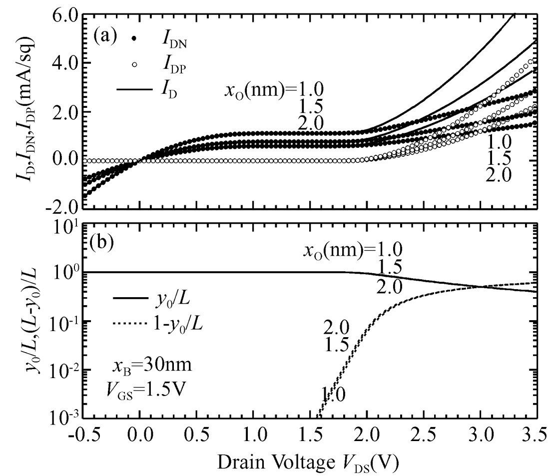

Fig. 9 Oxide thickness x_O dependence of the DC output current-voltage characteristics. The BiFET has two identical MOS gates on a thin pure base. x_B = 30nm, V_{GS} = 1.5V, V_{SB} = 0.0V. (a) The electron channel current I_{DN}, the hole channel current I_{DP} and the total drain current I_D. (b) The flatband line position y_0/L, the electron emitter section length y_0/L and the hole emitter section length $(L - y_0)/L$.

4.1 Current-Voltage Characteristics

Figure 3(a) gives the transfer current-voltage characteristics, namely, the electron channel current I_{DN} and the hole channel current I_{DP}, and the total channel current I_D ($= I_{DN} + I_{DP}$) or the drain terminal current, as a function of the gate terminal voltage, V_{GB}, (-2.0V to $+3.0$V) with the source terminal as the reference, V_{SB} = 0, and all the contact potential differences included in the terminal voltages (such as V_{FB} of the two identical gates), at three drain to source voltages, V_{DS} = 0.5, 1.0, and 2.0V.

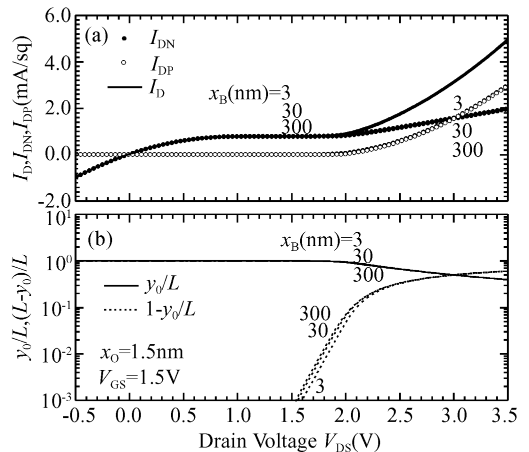

Fig. 10 Base layer thickness x_B dependence of the DC output current-voltage characteristics. The BiFET has two identical MOS gates on a thin pure base. x_O = 1.5nm, V_{GS} = 1.5V, V_{SB} = 0.0V. (a) The electron channel current I_{DN}, the hole channel current I_{DP} and the total drain current I_D. (b) The flatband line position y_0/L, the electron emitter length y_0/L and the hole emitter length $(L - y_0)/L$.

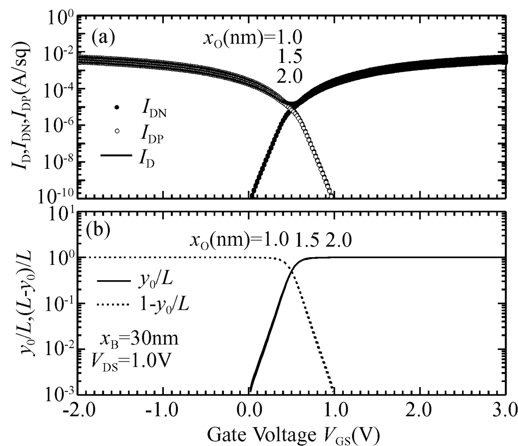

Fig. 11　Oxide thickness x_O dependence of the DC transfer current-voltage characteristics. The BiFET has two identical MOS gates on a thin pure base. $x_B = 30$nm, $V_{DS} = 1.0$V, $V_{SB} = 0.0$V. (a) The electron channel current I_{DN}, the hole channel current I_{DP} and the total drain current I_D. (b) The flatband line position y_0/L, the electron emitter section length y_0/L and the hole emitter section length $(L - y_0)/L$.

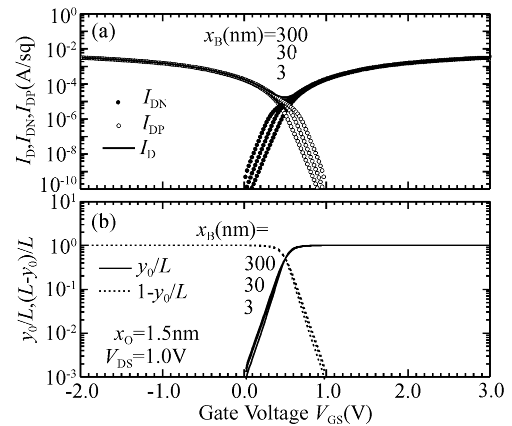

Fig. 12　Base layer thickness x_B dependence of the DC transfer current-voltage characteristics. The BiFET has two identical MOS gates on a thin pure base. $x_O = 1.5$nm, $V_{DS} = 1.0$V, $V_{SB} = 0.0$V. (a) The electron channel current I_{DN}, the hole channel current I_{DP} and the total drain current I_D. (b) The flatband line position y_0/L, the electron emitter length y_0/L and the hole emitter length $(L - y_0)/L$.

Figure 3(b) gives the length, y_0, of the electron-emitting source section which is also the length of the hole-collecting source section, and the length, $L - y_0$, of the drain hole emitter section, which is also the length of the drain electron collector section. Note the sharp change when the second channel (hole or electron) start to appear, or y_0/L or $1 - y_0/L$, started to change sharply from 1. The y_0 variation also marks the onset of increasing deviation of the 50% unipolar theory, used by all recent and past theorists, from our new and complete, 100%, bipolar theory, presented here. From these figures, it is evident that the deviation becomes large at the threshold voltage and in the subthreshold range.

Figures 4(a) and 4(b) give the output current-voltage and electrical-channel-section-length-voltage characteristics, similar to the transfer characteristics of Figs. 3(a) and 3(b), except that here in Figs. 4(a) and 4(b), the drain-to-source terminal voltage, V_{DS}, is the independent variable, instead of V_{GS} of Figs. 3(a) and 3(b).

The transconductance and output conductance versus drain or gate voltages are graphed in Figs. 5(a), 6(a), 7(a) and 8(a), and the corresponding channel section lengths, y_0 and $L - y_0$, in Figs. 5(b), 6(b), 7(b) and 8(b), which also give their derivatives with respect to the voltages, since the derivatives appear in the analytical solutions of the conductances indicated in Eqs. (3) and (4) of Ref. [12]. The variations are self-explanatory based on device physics already given in the first article of this series[12] so further elaboration is not needed.

4.2　Gate-Oxide and Base-Channel Thickness Dependences

Figures 9(a) and 9(b) give respectively the oxide thickness dependence of the output current-voltage characteristics, I_D versus V_{DS}, and the channel section lengths, y_0 and $L - y_0$ versus V_{DS}.

Figures 10(a) and 10(b) give respectively the base-thickness dependence of the output current-voltage characteristics, I_D versus V_{DS}, and the channel section lengths, y_0 and $L - y_0$ versus V_{DS}.

Figures 11(a) to 12(b) give the oxide and base thickness dependence of the transfer current-voltage characteristics, I_D versus V_{GS}, and the channel section lengths, y_0 and $L - y_0$ versus V_{GS}.

4.3　Deviations of the Long Channel Solution From the Short Channel Solution

Figures 13 and 14 give respectively the deviations of the long channel solution of the BiFET theory [12] from the short channel solution of the BiFET theory versus the gate and drain voltages. In the long channel solution, the channel section lengths are taken as the physical base-channel-base length, L, not taking account of the shorten electrical lengths of both electron and hole emitters.

5　Summary

The electrically short channel is an universal intrinsic property of all field-effect transistors (FET). This has not been recognized for 55 years since the invention of the FET by Shockley in 1952[4], although electrically short channel was indeed taken into account by Shockley[4] and by Prim and Shockley in a

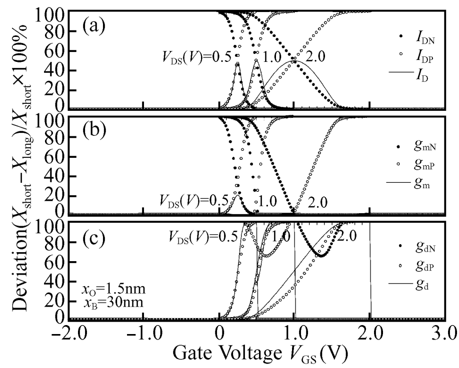

Fig.13 Deviations of the long channel solution (X_{long}) of the BiFET theory from the short channel solution (X_{short}) versus the gate voltage. The BiFET has two identical MOS gates on a thin pure base. (a) The electron channel current I_{DN}, the hole channel current I_{DP} and the total drain current I_D; (b) The total transconductance g_m, its electron component g_{mN} and its hole component g_{mP}. (c) The total output conductance g_d, its electron component g_{dN} and its hole component g_{dP}.

detailed mathematical analysis[5] of the junction-gate FET (JGFET). The present paper takes into account of the electrically short channel, using Shockley's original two-section idea of his closer-to-one-dimensional JGFET for the highly two-dimensional insulated-gate FET (IGFET) or MOS-gate FET (MOSFET). The unique feature or trick for analyzing the MOSFET is to recognize the presence of an intrinsic electrical boundary that separates the MOSFET into two electrical sections, namely the flatband line or plane when the drain voltage is equal or higher than the gate voltage (initially electron surface channel), where the x-component of the electric field vanishes, or where a constant electric field line or plane exists at a lower drain-source or a higher gate-source voltage. In the simple case of rectangular geometry with spatially constant impurity concentration, either one gate or the two gates treated in this paper, this boundary surface is a plane. For transistors asymmetrical in geometry or applied voltages, such a flatband boundary also exists as a general surface[7], no longer

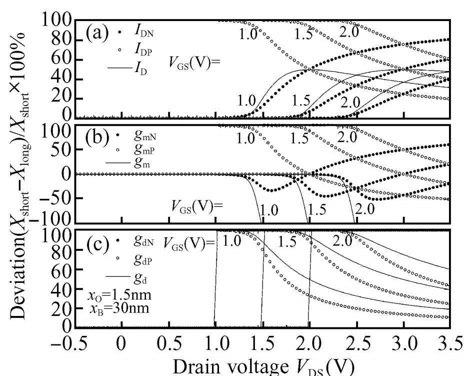

Fig. 14 Similar to Fig. 13, except versus drain voltage.

a plane. The electrical channel length of the two sections, y_0 and $L - y_0$, are computed from analytical formulas. They are also included in the channel current calculations to show that the shortened electrical channels indeed increase the current of the two surface channels from the two carrier species. In this paper, we also report the deviations of the channel currents from not taking account of the shortened electrical channels, which are important for compact modeling for shortening the computation times in circuit designs.

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双极场引晶体管:III.短沟道电化电流理论(双MOS栅纯基)*,**

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摘要：本文描述双极场引晶体管(BiFET)短沟道理论.晶体管分成两个区域，源区和漏区.每区在特定外加端电压下既可为电子或空穴发射区又可为电子或空穴收集区.把两维无缺陷Shockley方程分离为两个以表面势为参变量的一维方程，并运用源区和漏区界面处电子电流和空穴电流连续性，得到在源区和漏区内解析方程.典型BiFET包括薄纯基上两个等同金属氧化物硅(MOS)栅.用图形提供实用硅基和氧化层厚度范围内，随直流电压变化，输出和转移电流和电导总量，电子沟道与空穴沟道分量，和两区电学长度.报道前没考虑沟道缩短的偏差.

关键词：双极场引晶体管理论；MOS场引晶体管；同时并存空穴电子表面沟道和体积沟道；表面势；短沟道理论；双栅纯基

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