Characterization of Gate Dielectric Using Oxides Generated by *in situ* Steam Generation

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Abstract: A new process for gate dielectric fabrication named *in situ* steam generation (ISSG) is reported. Based on the Deal-Grove model, an oxidation mechanism is proposed to break the Si－Si bond by an active atomic O and form a Si－O－Si bond during the oxidation process. The breakdown characteristics are investigated through a MOS-capacitor for both ISSG and furnace wet oxidation. The gate dielectric material generated by ISSG oxidation has a superior electrical performance owing to sufficient oxidation of weak Si-Si bonds relative to furnace wet oxidation, indicating a promising application in sub-micron IC device manufacturing.

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1 Introduction

Silicon dioxide has been used as a gate dielectric and isolation in integrated circuits over the past 30 years. As a consequence of its importance and the criticality of gate breakdown, a great deal of experimental work has been done to improve the electrical characteristics of gate dielectrics. Traditionally, gate oxides are usually grown in a high-temperature (around 700～1000℃) furnace with an atmospheric-pressure oxygen ("dry oxidation") or steam ("wet oxidation") ambient. In these oxidation processes, oxidants such as oxygen or H_2O molecule diffuse through the growing oxide to react at the propagating SiO_2/Si reaction interface. The Deal-Grove reaction-diffusion model[1] could provide a general description for the growth mechanism of this oxide.

Dielectric breakdown and oxide interface charge trapping are considered as limits for thin oxides. They seem to be determined from insufficient Si－O networks and H-related carrier traps[2]. In order to overcome these serious issues, an *in situ* steam generation (ISSG) process has been developed for gate dielectric growth with *in situ* to the combining of H_2 and O_2 gases occurring within the close vicinity of the wafers. Recent experiments for gate-oxide formation show that there are significant benefits to the ISSG process. During ISSG oxidation, lean premixed hydrogen and oxygen are introduced into a rapid thermal processing (RTP) reactor in which a wafer is radiantly heated to a preset temperature. At this temperature, the combustion is induced in close proximity to the silicon surface. The reaction between H_2 and O_2 produces not only steam (H_2O), but also by-products such as active atomic oxygen (O^*)[3]. It takes only a few seconds to form a thin oxide.

In this paper, temperature effects on oxidation are examined. The corresponding oxidation kinetics is discussed in detail. Then, the breakdown tests, including intrinsic and extrinsic characteristics, are carried out. We show that the samples generated by ISSG oxides have higher electrical reliability than those by the furnace wet oxide due to the sufficient oxidation of weak Si—Si bonds.

2 Experiment

2.1 Sample preparation

All experiments (see Table 1) were performed on 200mm p-type Ar annealed silicon (100) wafers. The wafers were treated by a standard RCA-cleaning followed by HF dipping and rinsing in deionized water. The ISSG oxidation and N_2 anneal process were carried out in an AMAT Centura system, as shown in Fig. 1. The RTP Centura, used for the oxidation of the samples, is a cold-walled reactor (the process chamber walls are water cooled). The wafer surface and the edge ring are the only hot surfaces and serve as pri-

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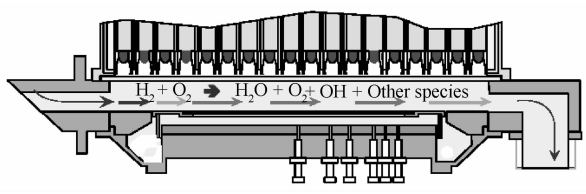

Fig. 1　Cross-sectional drawing of wet RTO process reactor

mary reaction sites. During the ISSG oxide growth, H_2 and O_2 directly flow across a rotating wafer heated by tungsten-halogen lamps. The hot wafer surface acts as an ignition source and the reaction between H_2 and O_2 occurs at the surface. This reaction produces oxidants such as atomic oxygen, H_2O, and other additional products. The atomic oxygen is considered to be responsible for the superior properties of the resulting SiO_2. Moreover, the strength of the built-in compressive strain near the Si/SiO_2 interface is reduced when processing at high temperature and/or in a steam ambient.

The entire experiment included both growth characteristics and electrical characteristics. The growth characteristics mainly focused on the temperature effect on ISSG growth. The electrical characteristics employed the constant current stress (CCS) and time dependent dielectric breakdown (TDDB) tests for characterization, which will be detailed in the next section. For electrical characterization, two sets of process split conditions have been designed (as shown in Tables 1 and 2). Set 1 is for comparison between different oxides formed by both ISSG oxide and furnace wet oxide. Also, the effects on electrical characteristics of N_2 post-oxidation anneal (POA) or mixed N_2 dilute gas have been checked in this set. In set 2, all oxides have been generated by ISSG with a range of temperature from 900 to 1000℃, or an O_2 : H_2 ratio from 9.8 : 0.2 to 9 : 1.

Table 1　Process split for sample preparation (set 1)

Sample No	Description	Condition	Optical thickness/nm
1	Furnace wet oxidation	Furnace wet oxide (850℃/O_2 10slm/H_2 10slm)	6.52 ± 0.02
2	ISSG oxidation + POA N_2	ISSG oxide (1050℃/O_2 9.8slm/H_2 0.2slm) + POA N_2 (1100℃/N_2 10slm/300s)	6.47 ± 0.02
3	ISSG oxidation	ISSG oxide (1050℃/O_2 9.8slm/H_2 0.2slm)	6.46 ± 0.03
4	ISSG oxidaion with N_2 dilute	ISSG oxide(1050℃/O_2 9.8slm/H_2 0.2slm/N_2 10slm)	6.51 ± 0.01

Table 2　Process split for comparison among ISSG oxides (set 2)

Sample No.	Description	Condition	Optical thickness/nm
5	ISSG oxidation	900℃/O_2 9.5slm/H_2 0.5slm	64.8 ± 0.01
6	ISSG oxidation	950℃/O_2 9.5slm/H_2 0.5slm	6.49 ± 0.01
7	ISSG oxidation	1000℃/O_2 9.5slm/H_2 0.5slm	6.52 ± 0.01
8	ISSG oxidation	950℃/O_2 9.8slm/H_2 0.2slm	6.53 ± 0.02
9	ISSG oxidation	950℃/O_2 9slm/H_2 1slm	6.52 ± 0.02

2.2　Physical and electrical measurement

The film optical thickness was characterized using the Rudolph ellipsometer with a refractive index of 1.46. The oxide quality was determined by the constant current stress and time dependent dielectric breakdown tests. All these tests were performed with n^+-polysilicon-gate MOS capacitors. The MOS capacitor structures were carried out using a patterned poly-Si film by LPCVD over a 6.5nm-thick gate oxide film. The structure and the process flow for the MOS-capacitor fabrication are shown in Figs. 2 (a) and 2 (b).

The breakdown test includes extrinsic and intrinsic characteristics. For the extrinsic breakdown characteristics, the test mainly monitors the defects (weak spot) in the oxides. The gate voltage (V_g) is measured after one-second current stress ($J_{stress} = -0.00025$nm/cm^2, medium region of F-N tunneling). The capacitor area A used to obtain the data about the cumulative probability plots was 10mm^2. The definition of failure is that V_g is less than 8.0V. D_0, the defect density in

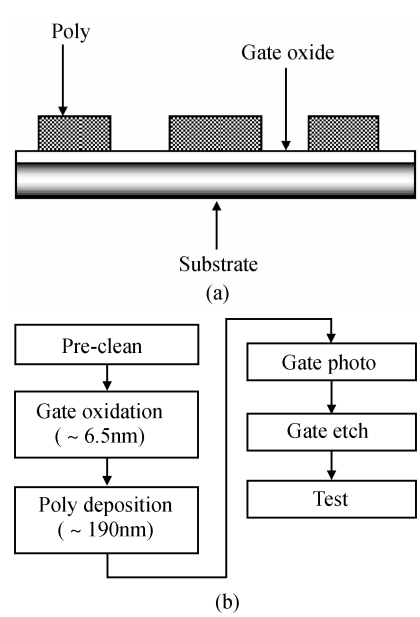

Fig. 2　(a) Structure of the MOS-capacitor for electrical breakdown characterization; (b) Process flow for the MOS-capacitor preparation

the area, is used to evaluate the extrinsic characteristics (defects). The defects are assumed to be uniformly distributed and can be calculated from the following formula[4] (As correct factors, 0.3 and 0.4 in this equation are based on the empirical statistics).

$$\exp(-D_0 A) = 1 - \frac{i - 0.3}{n + 0.4} \tag{1}$$

where i is the number of the failure sites and n is the quantity of the test site.

In this experiment, there are 190 test keys within each wafer, meaning that n equals 190. As for intrinsic characteristics, the gate voltage is continuously monitored until oxide hard-breakdown. The constant current density stressed at gate is $J_{\text{stress}} = 0.05\text{nm/cm}^2$. The capacitor area used is 0.05mm^2. A shift in V_g over 15% is identified as hard-breakdown. The 63.2%-charge-to-breakdown (Q_{bd}) (the charge quantity when 63.2% devices have failed) is used to evaluate the intrinsic breakdown characteristic. The etch rate test is introduced for the texture evaluation of the oxides. The solution used is mixed from 200 parts H_2O : 1 part 49% HF, by volume, at room temperature ($T \approx 23$℃).

3 Results and discussion

3.1 Temperature effect on ISSG growth

As indicated by Deal and Grove[1], the relationship of oxide thickness X and process time t can be expressed as:

$$X^2 + AX = B(t + \tau) \tag{2}$$

where

$$\begin{cases} A = 2D\left(\dfrac{1}{k_s} + \dfrac{1}{h}\right) \\ B = \dfrac{2D}{N_0} \times C^* \end{cases} \tag{3}$$

The quantity τ corresponds to a shift in the time coordinate that corrects for the presence of the initial oxide layer. D is the diffusion rate constant. k_s is the reaction rate constant. h is the gas phase mass-transfer coefficient. N_0 is the number of oxidant molecules incorporated into a unit volume of oxide. C^* is the equilibrium concentration in the bulk of the oxide.

From the above equation, the data on silicon oxidation can be evaluated using the parabolic rate law. The values of parabolic rate constant B and linear rate constant B/A are obtained as a function of temperature. Both rate constants follow an exponential dependence on temperature (Arrhenius behavior). The behavior of B with temperature, is expressed as

$$B = B_0 \exp(-E_a/kT) \tag{4}$$

where B_0 is the pre-exponential constant (which depends on C^* and N_0), E_a is the activation energy for the diffusion of O^* through SiO_2, k is the Bolzmann's constant, and T is the temperature.

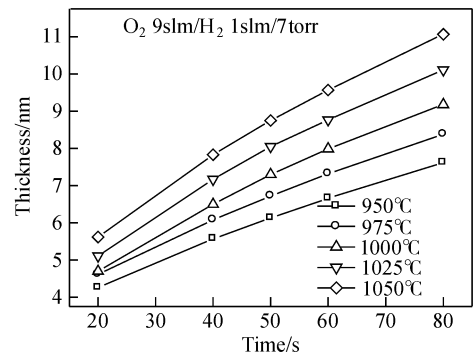

Fig. 3 Oxide thickness as a function of oxidation time at different temperatures (950～1050℃)

Table 3 Rate constants of the ISSG as a function of different temperature (950～1050℃)

Temperature/℃	A/nm	B /(nm²/s)	(B/A)/(nm/s)
950	2.26	0.722	0.32
975	2.3	0.835	0.36
1000	1.87	1.064	0.57
1025	1.56	1.22	0.78
1050	1.49	1.64	1.1

Figure 3 plots the thickness values of ISSG oxides as a function of oxidation time at various temperatures (950～1050℃), with a gas flow O_2 : H_2 = 9slm : 1slm. Table 3 shows the rate constants including A, B, and B/A in this temperature range. All these rate constants were obtained from parabolic curve fitting of the data plotted in Fig. 3 by the Origin software.

Figure 4 plots the natural log of parabolic rate constant B as a function of oxidation temperature. The activation energy, 1.124eV, for the diffusion of atomic oxygen in SiO_2 was obtained from the slope of the fitting line (slope $= -E_a/k$). This result is in accordance with the value provided by Bongiorno[5]. Meanwhile, the activation energy of atomic oxygen diffusing in oxide is lower than H_2O (for H_2O diffusion in silicon dioxide, $E_a = 0.8\text{eV}$[6]), implying that

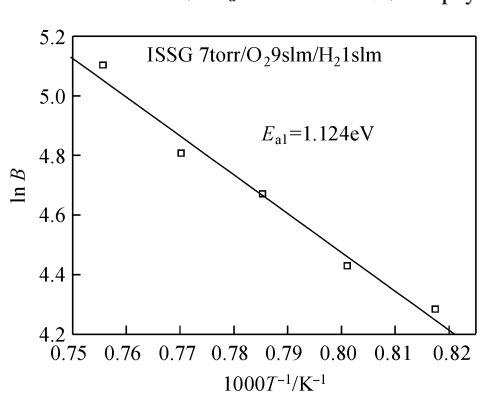

Fig. 4 ln$B$ as a function of oxidation temperature

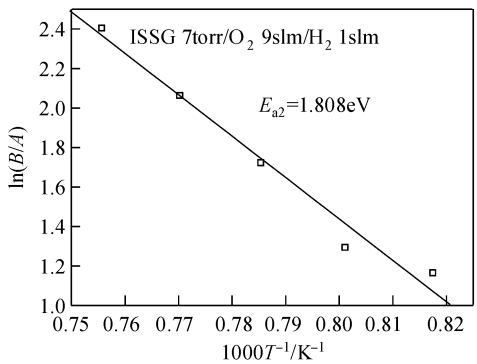

Fig. 5　$\ln(B/A)$ as a function of oxidation temperature

the diffusion of O^* in oxide is relatively more difficult than H_2O. Thus, we speculate that the ISSG oxidation in the thinner parts of the SiO_2 proceeds more slowly compared with the wet oxidation, achieving a smoother SiO_2/Si interface.

Figure 5 shows the temperature dependence of the linear rate constant (B/A) for ISSG oxidation. The reaction rate constant k_s is given by[6]

$$k_s = k_0 \exp(-E_{a2}/kT) \tag{5}$$

where k_0 is the pre-exponential constant, and E_{a2} is the activation energy required for reaction, which is sometimes associated with the reaction mechanism. Applying Eq. (5) to Eq. (3), we can obtain:

$$\frac{B}{A} = k_s \frac{C^*}{N_0} = k_0 \exp\left(-\frac{E_{a2}}{kT}\right) \times \frac{C^*}{N_0} = \left(\frac{B}{A}\right)_0 \exp\left(-\frac{E_{a2}}{kT}\right) \tag{6}$$

The activation energy calculated from the fitting line is 1.808eV. This is close to the energy required to break a Si—Si bond (1.83eV), indicating the Si—Si bond must break in order to form SiO_2. The proposed oxidation mechanism is presented in Fig. 6 to account for how a Si—Si bond is broken by an active atomic O and a Si—O—Si bond is formed. The reaction is:

$$O^* + Si—Si \rightarrow Si—O—Si \tag{7}$$

3.2　Etch rate

The etch rate test (see Fig. 7) shows that all oxides generated by the ISSG process exhibit lower etch rate than furnace wet oxide, indicating more compact texture within these oxides. Among all samples in set 1, sample ＃4 ("ISSG with N_2 dilute") showed the lowest etch rate, indicating that N_2 dilute gas gave rise to the most compact texture within bulk oxide. This texture feature could be correlated with the electrical properties.

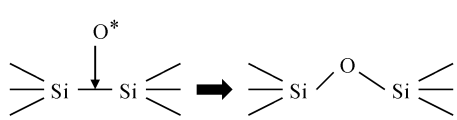

Fig. 6　A proposed oxidation mechanism for ISSG

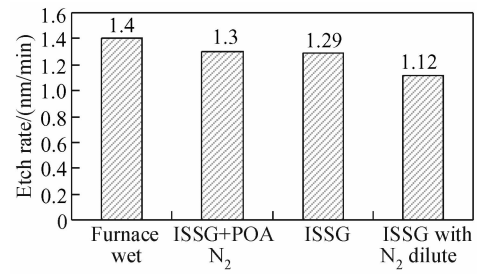

Fig. 7　Comparison of etching rate for ISSG and furnace wet oxides

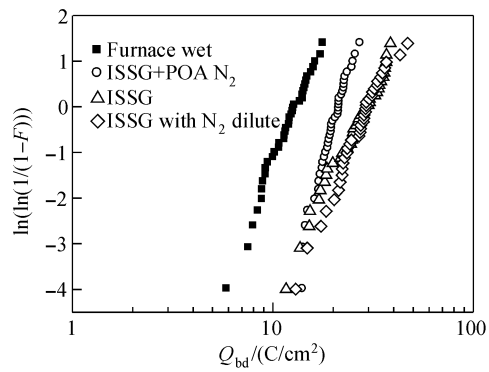

Fig. 8　Weibull plot of the charge-to-breakdown for MOS capacitors with furnace-wet and various ISSG oxides under constant current (0.05nm/cm²)　Capacitors with an area of 0.05mm² were used to obtain the "intrinsic" charge-to-breakdown. ISSG-forming oxides show significantly better oxide quality.

3.3　Electrical reliability test

Figure 8 shows the cumulative failure versus charge-to-breakdown (Q_{bd}) of samples (in set 1). The dielectric breakdown characteristics of the various ISSG oxides under the constant current stress are remarkably improved over that of the wet oxide. Figure 9 shows the D_0 calculated from Eq. (1) and charge-to-breakdown at cumulative failure of 63.2% (Q_{bd} (63.2%)) for all the samples (in set 1). A comparison on electrical characteristics can be made between these oxides: (1) The D_0 of ISSG oxides with various process conditions are around 30～50% less than that of wet oxide; (2) The Q_{bd}(63.2%) of the ISSG oxides with various process conditions, are around 60% ～ 130% higher than those for furnace wet oxides.

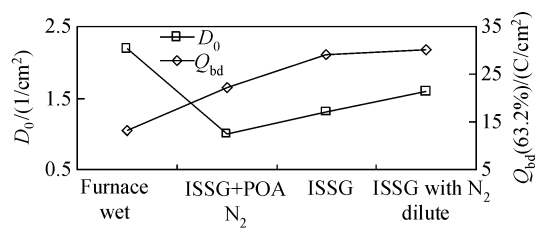

Fig. 9　Calculated defect density and 63.2%-charge-to-breakdown (Q_{bd}(63.2%)) for oxides formed under different conditions

A proposed mechanism to explain why the ISSG-formed oxides exhibit high resistance to breakdown over those formed in furnace is as follows. (1) Highly reactive O^* can repair the defects such as Si—Si bonds, silicon dangling bonds, strained Si—O bonds, and oxidize clusters of Si atoms at the SiO_2/Si interface. (2) Due to the low diffusion rate constant of O^*, the oxidation comes to slow down more quickly as the oxide thickness increases. This induces the O^* oxidation in thinner parts of the SiO_2 to proceed more rapidly, thus smoothing the interface. (3) The more compact texture formed with ISSG oxidation gives rise to a more robust oxide bulk. Also, a comparison of D_0 and charge-to-breakdown is finished for various ISSG processes based on the electrical test result above. The electrical performance is improved as temperature increases.

Based on the above results, several conclusions can be made: (1) The oxidation followed by a treatment of N_2 anneal reduces defect density, enhancing the resistance to extrinsic breakdown but degrading the intrinsic breakdown characteristics; (2) Process gas diluted with N_2 improves the intrinsic breakdown characteristics, but increases the defect density relatively.

The larger charge-to-breakdown of oxide is due to reduced charge trapping since the breakdown mechanism of gate dielectrics is generally accepted to be related to charge trapping within oxide[7]. In the oxidation model proposed above, we assumed that the Si—Si bond is broken and replaced by the Si—O—Si bond during the ISSG oxidation process. The Si—Si bond is weak and it can be either an electron trap or a hole trap[8]. It becomes an electron trap when it traps an electron[9]. Oxide breakdown occurs as soon as a critical density of neutral electron traps in the oxide is reached[10]. If it traps a hole, it becomes an E' center in oxides during a breakdown process. Therefore, the Si—Si bond in oxide could be an inducement to lead the oxide breakdown. For the traditional furnace wet oxide, the reaction mechanism is relatively more complex than ISSG. It is generally described as follows[11]: A rapid reaction occurs between the interstitial water molecules and Si—O bridges to form silanol groups (Si—OH). The reaction is

$$H_2O + Si—O—Si \rightarrow 2Si—OH \quad (8)$$

Then, the reaction occurs between the formed silanol groups and Si—Si bonds at the Si/SiO_2 interface to form Si—O bridges and hydrogen molecules. The reaction is

$$2Si—OH + Si—Si \rightarrow 2Si—O—Si + H_2 \quad (9)$$

From a comparison between the oxidation mechanisms of furnace wet oxidation and ISSG oxidation,

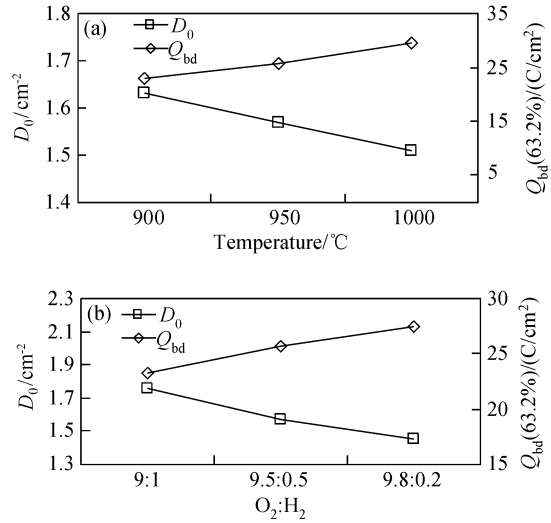

Fig. 10 (a) Calculated defect density and 63.2%-charge-to-breakdown of 6.5nm ISSG oxides as a function of temperature The ISSG oxides were grown with O_2 and H_2 (O_2 : H_2 = 9.5slm : 0.5slm); (b) Defect density calculated and 63.2%-charge-to-breakdown of 6.5nm ISSG oxides as a function of O_2 : H_2 gas flow ratio for ISSG-forming oxides with process temperature of 950℃

the oxidation with atomic O in ISSG [Eq. (7)] is a direct oxidation while the wet oxidation [Eqs. (8), (9)] is an indirect oxidation. The difference between oxidation mechanisms leads to different oxidation efficiency. As a result, ISSG gives rise to a relatively sufficient oxidation with respect to steam oxidation, meaning less Si—Si bonds exist after ISSG oxidation.

3.4 Temperature and gas flow ratio effect on electrical performance

Figure 10 (a) plots the defect density and the charge-to-breakdown (63.2%) as a function of oxidation temperature. Figure 10 (b) plots the defect density and the charge-to-breakdown (63.2%) as a function of O_2 : H_2 gas ratio. The following trends can be observed.

(1) The defect density decreased as the oxidation temperature increased (from 900 to 1000℃), as in the case of O_2 : H_2 = 9.5slm : 0.5slm. Meanwhile, the charge-to-breakdown increased in the same case as the oxidation temperature increased.

(2) The defect density decreased as the O_2 : H_2 gas flow ratio increased (from 9 : 1 to 9.8 : 0.2) at 950℃. Meanwhile, the charge-to-breakdown increased in the same case as the O_2 : H_2 gas flow ratio increased.

We speculated that the Si—H bonds in the oxide decrease as the concentration of H_2 is reduced among the mixed reaction gas. As the Si—H bond is such a weak bond, it is easily broken by the tunneling elec-

tron under the electrical stress and becomes a defect (e.g. silicon dangling bond) subsequently. The reduction of H_2 in mixed reaction gas gave rise to a positive effect on the electrical breakdown characteristics.

4 Conclusion

The excellent electrical properties of gate dielectric materials have been demonstrated by an ISSG oxidation process. The studies of the ISSG process show that it produces gate oxides with high quality and superior electrical reliability compared with traditional furnace wet oxidation. As indicated in the ISSG oxidation model, the Si—Si bond is broken by an active atomic O and then the Si—O—Si bond is formed during the oxidation process. The improvements in electrical breakdown characteristics are attributed to the sufficient oxidation of weak Si—Si bonds as a result of direct oxidation by the atomic O. As the breakdown of the gate dielectric is one of the major causes of circuit failure, the ISSG oxide is believed to be a promising candidate for more robust gate dielectric in the future IC fabrication.

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基于原位水汽生成工艺的栅氧化膜特性

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摘要：介绍了一种制作栅介质的新工艺——原位水汽生成工艺. 基于 Deal-Grove 模型提出了原位水汽生成过程中活性氧原子和硅—硅键反应形成硅氧硅键的氧化模型，并通过 MOS 电容结构对原位水汽生成和炉管湿法氧化所形成的栅氧化膜的电击穿特性进行了研究和分析. 测试结果表明原位水汽生成的栅氧化膜相对于炉管湿法氧化有着更为突出的电学性能，这可以认为是由于弱硅—硅键的充分氧化所导致的. 表明原位水汽生成在深亚微米集成电路器件制造中具有广阔应用前景.

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