Quasi-Static Energy Recovery Logic with Single Power-Clock Supply*

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Abstract: This paper presents a new quasi-static single-phase energy recovery logic (QSSERL), which unlike any other existing adiabatic logic family, uses a single sinusoidal supply-clock without additional timing control voltages. This not only ensures lower energy dissipation, but also simplifies the clock design, which would be otherwise more complicated due to the signal synchronization requirement. It is demonstrated that QSSERL circuits operate as fast as conventional two-phase energy recovery logic counterparts. Simulation with an 8bit logarithmic look-ahead adder (LLA) using static CMOS, clocked CMOS adiabatic logic (CAL, an existing typical single-phase energy recovery logic), and QSSERL, under 128 randomly generated input vectors, shows that the power consumption of the QSSERL adder is only 45% of that of the conventional static CMOS counterpart at 10MHz, and the QSSERL adder achieves better energy efficiency than CAL when the input frequency f_{input} is larger than 2MHz.

Key words: energy recovery; adiabatic logic; low power; digital CMOS; VLSI
EEACC: 1265A; 2560; 2570D
CLC number: TN432 **Document code**: A **Article ID**: 0253-4177(2007)11-1729-06

1 Introduction

Various energy recovery circuits (ERCs) with adiabatic circuitry for ultra-low power implementation have been reported in recent years[1~11]. Compared with conventional static CMOS circuits, they consume much less power. For instance, at 10MHz clock input, efficient charge recovery logic (ECRL)[3] dissipates only 16% of the energy of static CMOS logic in an inverter chain application. Clocked quasi-static energy recovery logic (CQSERL)[8] consumes only 35% in a 4bit carry ripple adder application. However, most of ERCs require a four-phase[1~4] or two-phase[5~8] power-clock. Multi-phase clocking brings several problems, such as a complicated clock tree design with clock skew, and increased energy dissipation with multiple power-clock generators.

Some logic families using single-phase power-clock have been presented[9~11]. Among them, clocked CMOS adiabatic logic (CAL)[9] is typical, which requires only one power-clock, which effectively simplifies the power-clock tree design. However, to ensure correct operation, it requires two additional timing control clocks, which results in a complicated timing control clock tree design and more energy dissipation. Another typical single-phase ERC family is pass-transistor adiabatic logic (PAL)[10]. Due to the requirement of two complementary sinusoidal power-clocks in its cascaded circuits, PAL is not a real single-phase based ERC.

In this paper, we propose a quasi-static single-phase energy recovery logic (QSSERL) family, which is a new logic without any additional timing control clocks. With its pure single power supply, QSSERL overcomes the drawbacks with other logic families mentioned above. In addition, due to its quasi-static nature, QSSERL does not need any data buffers to ensure the synchronization of signals that originate from different clock phases[11,12], which may otherwise cause extra power dissipation and area cost. We design and simulate an 8-inverter chain and an 8bit logarithmic look-ahead adder (LLA)[13] using QSSERL and compare them with their static CMOS and CAL logic implementations. Results show that QSSERL logic has the highest energy efficiency, especially at

* Project supported by the National Natural Science Foundation of China (No. 90307008)
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Received 2 June 2007, revised manuscript received 30 June 2007

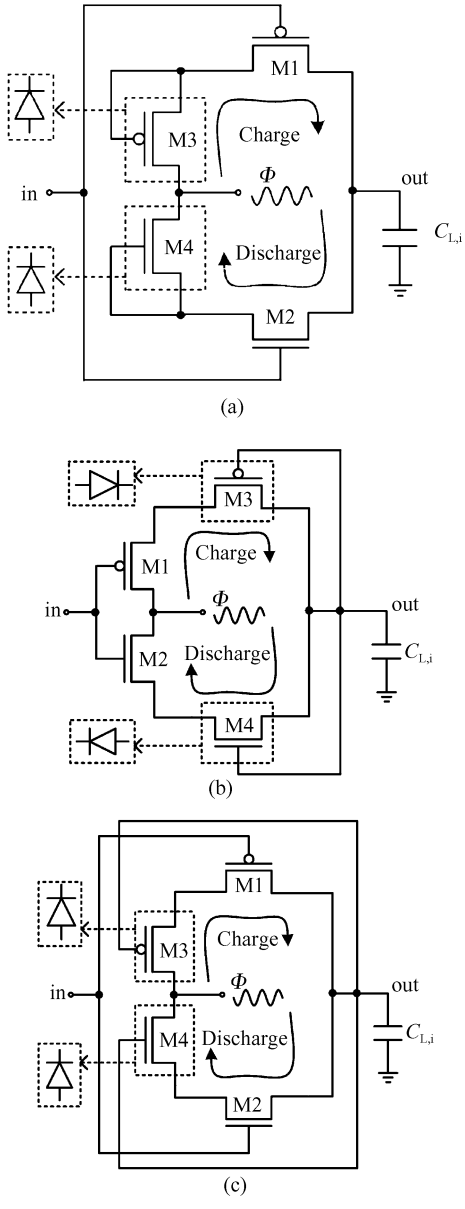

Fig. 1 (a) A QSSERL inverter where M3 and M4 function as two diodes; (b), (c) Another two possible ways to connect diodes

high input frequency ($f_{input}>2$MHz).

2 QSSERL

2.1 QSSERL inverter

The basic idea of QSSERL is explained with a QSSERL based inverter, as shown in Fig. 1 (a), where the capacitor $C_{L,i}$ represents the load and the transistors M3 and M4 are diode-connected to guide the current when charging or discharging $C_{L,i}$. The charging and discharging processes of Fig. 1 (a) are described as follows:

(1) Charging process: Initially, Φ is low and starts to rise. Both in and out are low, making a conducting path: $\Phi \rightarrow$M3$\rightarrow$M1$\rightarrow$out. Hence, out rises following Φ closely. Once out reaches $\Phi_{max}-|V_{th,p}|$, M3 cuts off. As long as in keeps low, M2 remains in the cut-off region. Thus, there is no conducting path between out and Φ. This makes out stay at high voltage regardless of Φ.

(2) Discharging process: Initially, Φ is high and starts to ramp down. Since both in and out are high, the conducting path becomes: out $\rightarrow$M2$\rightarrow$M4 $\rightarrow\Phi$. Hence, out decreases following Φ closely. As a result, little current flows toward the power source, Φ, which is recycling most of the energy previously stored on $C_{L,i}$. When out is reduced to $V_{th,n}$, M4 cuts off and out remains unchanged, no matter how Φ might change.

The output holds its state unless the input changes. Charging or discharging occurs only when the input changes its state (not necessarily every clock cycle, depending on the input frequency).

There are two other ways to connect the diodes M3 and M4, as shown in Figs. 1 (b) and (c). We do not use those connections for the following reasons:

(1) Connecting the gate of M3 and M4 directly to the out will introduce more capacitance at the output, which causes a great deal of power dissipation;

(2) The power-clock Φ will be coupled to the outputs of each stage in a cascaded circuit through both the gate-source capacitance of M1 and M2 in Fig. 1 (b) (M3 and M4 in Fig. 1(c)), causing a great deal of noise.

2.2 Multi-stage QSSERL circuits

A general structure for QSSERL-based combinational gates can be derived by replacing M1 with p-tree and M2 with n-tree, in which only two more transistors (M3 and M4) are needed than with static CMOS logic.

To illustrate how a QSSERL circuit works under one power-clock, we take the 4-stage circuit shown in Fig. 2 as an example. If an output of a certain stage in Fig. 2 is evaluated to be effective,

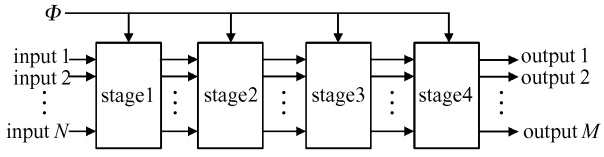

Fig. 2　A 4-stage QSSERL circuit where only one sinusoidal clock is required

it will be called "valid". And if this output is logic high (or low), it will be "valid-1" (or "valid-0").

Therefore, by following the operation principle of QSSERL that is described in section 2.1, it can be derived:

(1) Valid-1 output is the result of both valid-0 inputs with an ascending period of Φ;

(2) Valid-0 output is the result of both valid-1 inputs with a descending period of Φ.

Figure 3 illustrates the operation of the 4-stage QSSERL circuit. Assuming inputs $1 \sim N$ are all valid at t_0, the 1st stage produces its valid-1 and valid-0 outputs at time t_1 and t_2, respectively. At t_2, the 2nd stage produces its valid-0 output. Similarly, valid-1 outputs of the 2nd and 3rd stage are both produced at t_3, while valid-0 outputs of the 3rd and 4th stage are both produced at t_4. Outputs $1 \sim M$ are all valid at t_5, as both valid-0 and valid-1 outputs of the 4th stage are produced. Thus, the total time needed for data to pass through the 4-stage circuit is $5T/2$, where T is the period of Φ. In general, for an N-stage circuit, we can obtain

$$t_{\text{total}} = (N + 1)T/2 \tag{1}$$

When $N \gg 1$,

$$t_{\text{total}} \approx NT/2 \tag{2}$$

These equations imply that QSSERL circuits can operate as fast as two-phase ERCs.

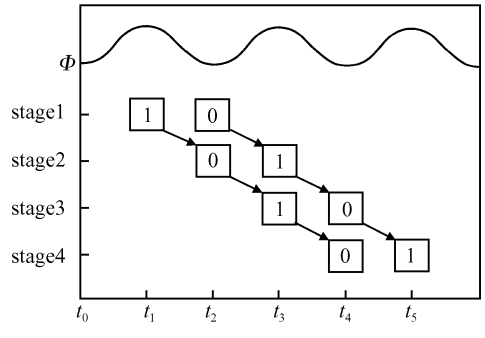

Fig. 3　Operation of the 4-stage QSSERL circuit, where "1" and "0" denote valid-1 and valid-0 outputs of a certain stage

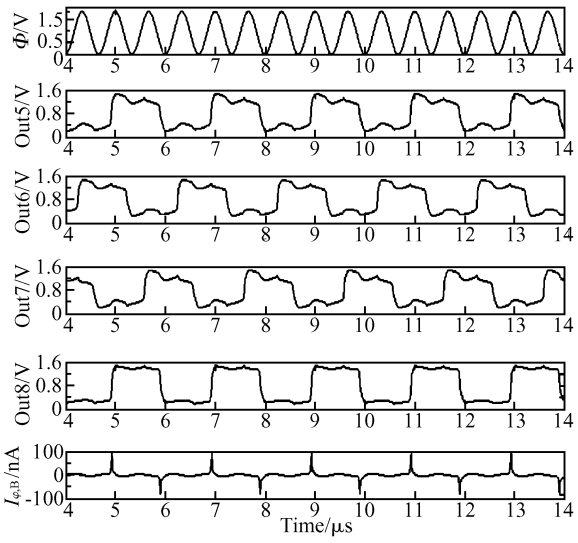

Fig. 4 Waveforms obtained from HSPICE simulations with the 8-inverter chain of Fig. 5　From top to bottom: (a) Power-clock Φ; (b) ~ (e) Output of the 5th stage to 8th stage; (f) Current of the 8th stage

3　Simulation results

We have designed and simulated an 8-inverter chain and an 8bit LLA using QSSERL, CAL, and static CMOS. The performance was verified through an HSPICE simulator, using SMIC 0.18μm standard CMOS technology. A 1.8V peak-to-peak sinusoidal voltage supply was used as the power-clock Φ throughout our simulation. All load capacitors of outputs were assumed to be 2fF.

In order to fairly compare the energy efficiency of QSSERL, CAL and static CMOS, we have optimized the transistor size of each circuit style to achieve the least energy consumption. Results show that all transistors should be the minimum size, because minimum transistor size leads to minimum node-capacitance, which ensures minimum energy consumption.

3.1　8-inverter chain

Figure 4 shows the simulation results of a QSSERL 8-inverter chain that are obtained when a periodic sequence "… 0101 …" was propagated through the inverter chain at 10MHz.

The outputs of the 5th stage to the 7th stage show some noise because there is no direct path from a certain stage's output to the power supply or ground for certain time intervals. This floating

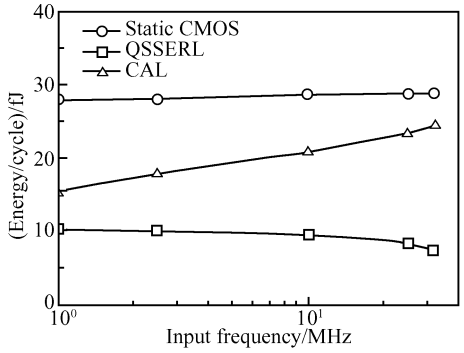

Fig. 5 Simulation results for energy consumption of 8-inverter chain with different logic implementations

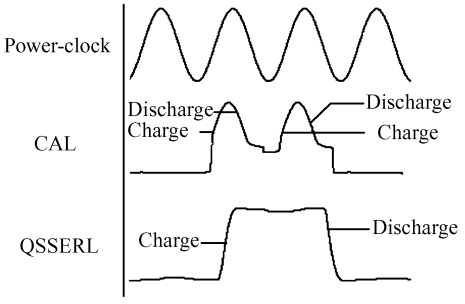

Fig. 6 Logic '1' generated by CAL and QSSERL

situation makes internal nodes susceptible to noises. For example, the power-clock Φ is coupled to the output of each stage due to clock feedthrough. However, with a load capacitor, the output of the 8th stage shows a stable waveform. Thus, a proper capacitor can be used at each output of the QSSERL circuit to obtain good voltage stability. Since this capacitor is only needed at the output of the whole circuit, the increased power consumption is tiny. The current of the 8th stage, $I_{\Phi,8}$, shown in Fig. 4, reveals an essential operation within any ERC circuit.

Figure 5 shows the comparison of energy dissipation of the 8-inverter chain with static CMOS, CAL, and QSSERL. To ensure operation, the power-clock frequency in CAL is assumed to be twice as much as its input frequency. At low frequency, both CAL and QSSERL show great energy savings compared with static CMOS, with QSSERL consuming the least energy. For instance, at 1MHz, CAL and QSSERL consume 59% and 40%, respectively, of the energy of the static CMOS. However, at high frequency ($f_{\text{input}} > 10$MHz), the energy consumption of CAL is very close to that of static CMOS. But QSSERL shows great energy savings at high frequency, consuming only 26% of the energy of the static CMOS at 32MHz.

Circuit nodes are necessarily charging and discharging every clock cycle in CAL. This dynamic nature leads to a lot of switching activity, which increases power dissipation. Figure 6 shows how logic '1' is generated by CAL and QSSERL, respectively. CAL needs two periods of charging and discharging, while QSSERL only needs one. This ensures less power dissipation for QSSERL. Additionally, the parasitic capacitance of internal nodes in QSSERL is smaller to those in CAL. For example, in QSSERL, an output of a certain stage connects two drains and two gates of adjacent transistors while it connects three drains and three gates in CAL. This also contributes to the high energy efficiency of QSSERL. Nevertheless, QSSERL consumes more power when the input frequency goes low, because the logic '1' is floating longer which introduces more noise, causing extra power consumption. CAL consumes more power when the input frequency goes high, due to power dissipation in the increased error voltage between logic trees. Thus, we believe that QSSERL is better used for high-frequency applications.

3.2 Logarithmic lookahead adder

In order to evaluate the energy efficiency of QSSERL in real applications, we also designed and simulated an 8bit LLA[13] using static CMOS, CAL, and QSSERL, as shown in Fig. 7 where a pipeline structure was used to ensure high throughput. To generate inverse signals, both QSSERL and static CMOS require inverters that are marked by broken lines in Fig. 7. But those inverters are not needed in CAL, because CAL is a dual-rail logic. Static CMOS needs all the inverters except those used in the pipeline. For CAL, in order to lower the energy consumption of timing control voltages, the amplitudes of the voltages were reduced to 0.9V, which is the minimum value to ensure operation.

A simulation was performed using 128 randomly generated input vectors, which were independent of one another. The probability of being HIGH for each input in an addition operation was assumed to be 0.5. The results are plotted in Fig. 8, where great energy savings of adiabatic circuits over static CMOS are shown again. As the input frequency increases, the energy consumption of CAL increases slightly. But QSSERL decreases

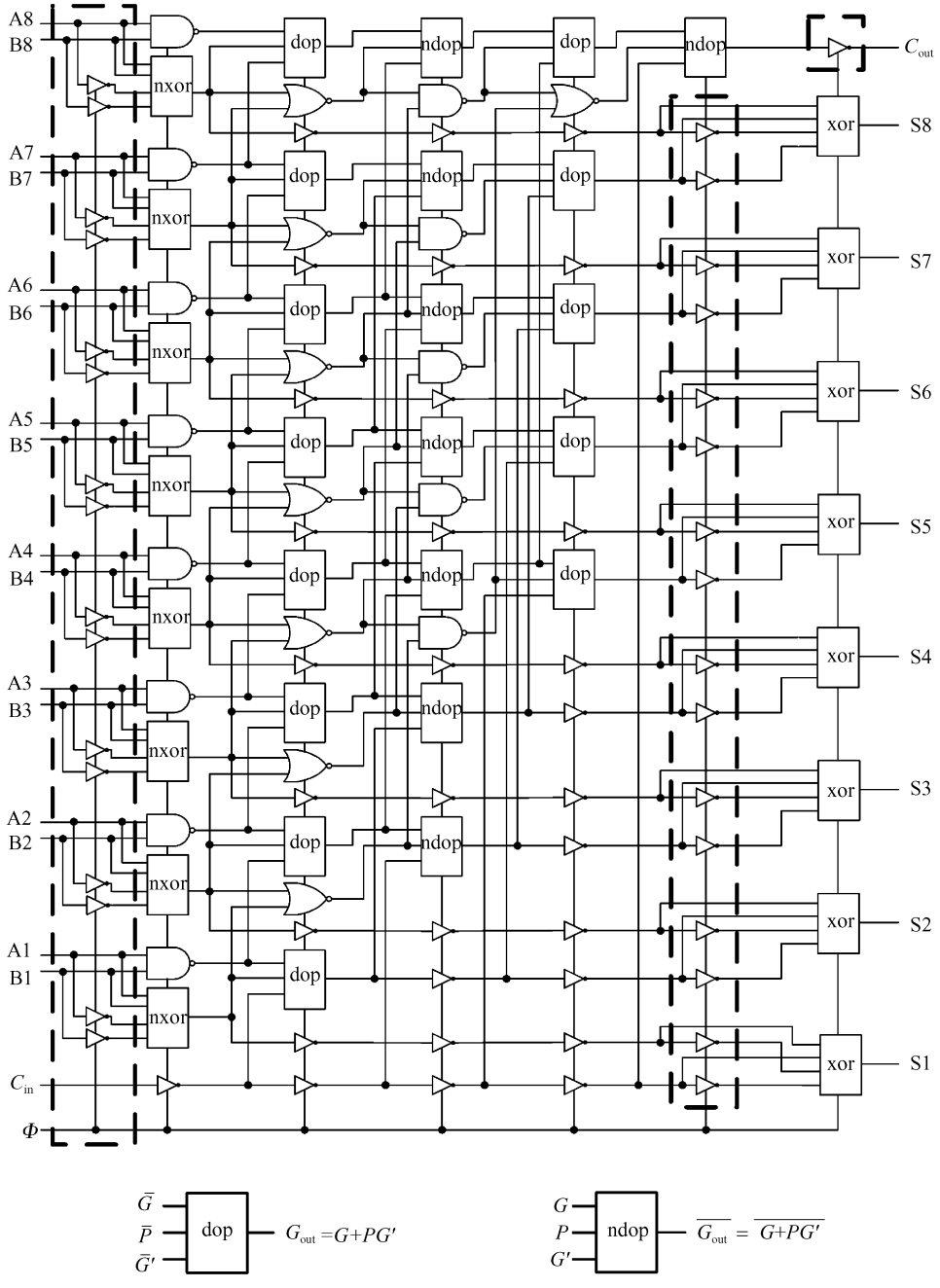

Fig. 7　Schematic of an 8bit LLA

due to the decreased energy consumption due to noise, as described in section 3.1. In particular, at 1MHz, QSSERL saves 48% of the energy used by static CMOS, while CAL saves 54%, which is slightly more than QSSERL. At 2MHz, both QSSERL and CAL save approximately 52%. When the frequency reaches 12.5MHz, QSSERL saves 55%, while CAL saves only 37%. Therefore, QSSERL is more power efficient than CAL for this adder implementation at high frequency ($f_{input}>$ 2MHz). Also, it should be emphasized that QSSERL needs only one power-clock without any auxiliary timing control voltages, which significantly simplifies the clock design.

4　Conclusion

We have presented QSSERL, a low-power quasi-static energy recovery logic with a true single-phase power clock. The quasi-static nature of this logic leads to less switching activity and low power consumption, while the single-phase power-

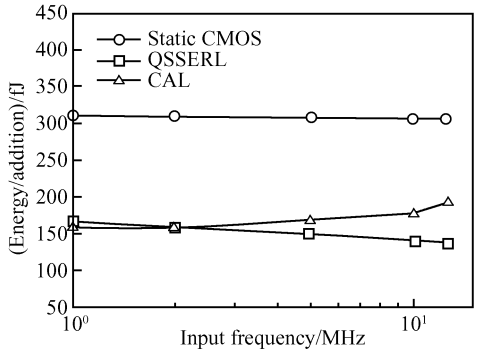

Fig. 8 Simulation results for energy consumption of logarithmic lookahead adders

clock makes it easier to design the clock network for synchronous systems. Compared with the existing single-phase based logic family (CAL), QSSERL not only consumes less energy at high input frequency ($f_{\text{input}} > 2\text{MHz}$), but also requires no auxiliary timing control clocks. It has also been demonstrated that this logic can operate as fast as two-phase power-clock based energy recovery logic.

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准静态单相能量回收逻辑*

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摘要: 提出了一种新的准静态单相能量回收逻辑,其不同于以往的能量回收逻辑,真正实现了单相功率时钟,且不需要任何额外的辅助控制时钟,不但降低了能耗,更大大简化了时钟树的设计.该逻辑还可以达到两相能量回收逻辑所具有的速度.设计了一个 8 位对数超前进位加法器,并分别用传统的静态 CMOS 逻辑、钟控 CMOS 绝热逻辑(典型的单相能量回收逻辑)和准静态单相能量回收逻辑实现.采用 128 组随机产生的输入测试向量的仿真结果表明:输入频率为 10MHz 时,准静态能量回收逻辑的能耗仅仅是传统静态 CMOS 逻辑的 45%;当输入频率大于 2MHz 时,可以获得比时钟控 CMOS 绝热逻辑更低的能耗.

关键词: 能量回收; 绝热逻辑; 低功耗; 数字 CMOS; 超大规模集成电路

EEACC: 1265A; 2560; 2570D

中图分类号: TN432 **文献标识码:** A **文章编号:** 0253-4177(2007)11-1729-06

* 国家自然科学基金资助项目(批准号:90307008)

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2007-06-02 收到, 2007-06-30 定稿