Improvements on High Current Performance of Static Induction Transistor

Wang Yongshun†, Wu Rong, Liu Chunjuan, and Li Siyuan

(*School of Electronic and Information Engineering, Lanzhou Jiaotong University, Lanzhou 730070, China*)

Abstract: Methods for improving the high current performance of static induction transistor (SIT) are presented. Many important factors, such as "trans-conductance per unit channel width" θ, "gate efficiency" η, "sensitivity factor" D, and "intrinsic static gain" μ_0, that may be used to describe different aspects of the electrical performance of an SIT are first defined. The dependences of electrical parameters on the structure and technological process of an SIT are revealed for the first time. The packaging technologies are so important for the improvement of high power performance of SITs that they must be paid attention. Testing techniques and circuits for measuring frequency and power parameters of SITs are designed and constructed. The influence of packaging processes in technological practice on the electrical performance of SITs is also discussed in depth.

Key words: static induction transistor; gate efficiency; intrinsic static gain; sensitivity factor
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1 Introduction

In recent years, a large quantity of research on static induction transistors (SIT) has been done for high power and high frequency applications[1~8]. One of the main advantages of the SIT device is its large current capability[3,4]. As a high power device, an SIT needs to resist high voltage with a small leakage current in the reverse blocking state and to conduct a large current with a small voltage drop in the forward conducting state. Unfortunately, these two needs are contradictory in structure and fabrication process. This issue can only be coped with by means of some trade-offs between the two needs. The superior high current performance indicates that an SIT has a high capability of conducting a large current and a high sensitivity for both gate voltage V_G and drain voltage V_D to control the current flowing from source to drain. In other words, small variations of V_G and V_D can result in a large change of drain current. While the output current may be raised by increasing the area of the active region, or increasing the number of channels N_c, the stripe width of unit channel W_c and the channel thickness d_c, this approach is still constrained by many factors such as operating frequency, breakdown performance, the state of technology, and thermal dissipation. As a consequence, the effective method to increase output current is to increase the capability of output current and the sensitivity of controlling current, which are characterized by the parameters of trans-conductance g_m and drain conductance g_d.

2 Device structure

SIT samples used to measure the high current performance are fabricated using a buried gate structure. The channel, source, drain and gate are doped at impurity concentrations of $N_{DC} = 10^{14}$ cm^{-3}, $N_{DS} = 10^{19}\,cm^{-3}$, $N_{DD} = 10^{19}\,cm^{-3}$, and $N_{AG} = 10^{19}\,cm^{-3}$, respectively. The channel length $L_D = 750\mu m$, gate length $L_G = 8\mu m$, gate-to-gate space is $9\mu m$, and the repeated period is $25\mu m$. The channels and gate stripes are alternately arranged, making it convenient to place many units in parallel in a single SIT. In order to estimate the high current performance of an SIT and to obtain critical design rules and processing information, testing techniques and systems are established on the basis of the operating mechanism for high power measurements.

† Corresponding author. Email: wangysh@mail.lzjtu.cn
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Table 1　Trans-conductance comparisons between a single cell and its parallel combinations

No.	BV_{GDO}/V	BV_{GSO}/V	g_m/mS	$-V_p$/V	Amount
1 single	95	7.8	20	3.0	1
2 single	95	7.0	15	2.0	1
3 single	80	8.2	12	2.5	1
1,2 parallel	85	6.8	50	1.5	2
1,2,3 parallel	72	6.8	62	1.7	3

3　Combination feature of trans-conductance g_m

An SIT consists of a multi-unit with parallel multi-channels. The trans-conductance g_m is a comprehensive parameter representing the performance of the total structure. The experimental comparisons between one cell with the number of channels $N_c = 140$, the length of a channel $d_c = 180\mu m$, and its two or three parallel combinations are illustrated in Table 1.

From Table 1, it is apparent that the total g_m is obviously increased after they are connected in parallel, even larger than the sum of their respective single values. With the increasing of the number of cells connected in parallel, the values of BV_{GDO}, BV_{GSO}, and V_p of the combined devices of three cells are decreased 20%, 6%, and 30% of the average value of their single cells, respectively. Hence, in order to increase g_m, the method of parallel connection of many cells with some trade-off to BV in an acceptable range is utilized. This is a feasible technological approach to increase g_m.

4　Trans-conductance per unit channel width θ

For accurately estimating the capability of providing trans-conductance for various SITs, the trans-conductance per unit channel width θ is first defined as $\theta \equiv g_m / W$, where W is the total width of all channels $W = N_c W_c$. The significance underlying θ can be clearly seen from the experimental data in Table 2.

Table 2　Trans-conductance per unit channel width for different SITs

No.	g_m/mS	W/cm	$\theta = g_m W^{-1}$/(mΩ · cm^{-1})
T1	169	7.32	23
T2	160	6.93	23
T3	160	7.11	22.5
T4	70	1.54	45.5
T5	220	4.60	47.8

The unit channel width may have different trans-conductance g_m for the same SIT, reflecting the matching relationship among the geometrical dimensions, the structural feature, the fabrication process and the material used to manufacture the SIT. If the value of θ is used to evaluate the performance of SITs listed in Table 2, it is obvious that although devices T1, T2 and T3 have relatively large width W, the values of their θ are small, showing that the SIT has a low ability to output current. The devices T4 and T5 have high values of θ, indicating that the ability to output current is much superior. To improve the trans-conductance g_m, one approach is to increase the channel width W. Usually the ratio of channel width to its length (W/l_c) is considered as a design parameter. In order to obtain large g_m and conduct high current, it is an effective method to increase the value of W/l_c. For example, given $l_c = 2.5\mu m$, the values of the ratio W/l_c of T1, T2, and T3 are 2.928×10^4, 2.772×10^4, and 2.844×10^4, respectively. It seems that the first three SITs in Table 2 should have large g_m values and a high ability to output current. But because of small θ, the trans-conductance g_m is rather low. Therefore, it is important to improve the trans-conductance per unit width θ, reflecting the capability of conducting high current.

5　Critical approaches to improving trans-conductance

According to the definition:

$$g_m \equiv \left.\frac{\partial I_D}{\partial V_G}\right|_{V_D = \text{const}} \approx \left.\frac{\Delta I_D}{\Delta V_G}\right|_{V_D} \qquad (1)$$

The trans-conductance reflects the magnitude of the current change caused by the variation in gate voltage V_G, i.e., the control sensitivity of V_G to the drain current. In the case of an SIT, g_m represents the control sensitivity of V_G to the potential barrier (including height, width and position), which modulates the injection of carriers towards the drain electrode. By simple theoretical analysis, the sensitivity can be expressed in terms of "gate efficiency":

$$\eta = \frac{\partial \phi_{min}(V_G V_D)}{\partial V_G} \approx 1 - 2\mu_0^{-1/2} \qquad (2)$$

where $\mu_0 \equiv \exp\left(\pi \frac{l_c}{d_c}\right) > 1$ is defined as the intrin-

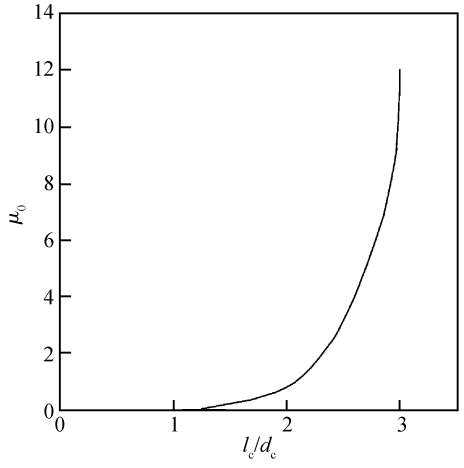

Fig. 1 Intrinsic static gain μ_0 versus l_c/d_c

sic static gain describing the controlling ability of the drain voltage to the potential barrier in the channel, compared with the gate voltage. The gate efficiency η is the voltage amplification coefficient of the SIT corresponding to that of a vacuum triode. The larger the gate efficiency η is, the more sensitively the gate voltage controls the potential barrier (and hence the drain current). The gate efficiency η and intrinsic electrostatic gain μ_o are approximately determined only by the geometric parameter l_c/d_c of the device. For a given length of the channel, the reduction in thickness d_c is an effective step to enhance the controlling ability of the gate voltage to the potential barrier. The dependences of μ_0 and η on l_c/d_c are shown in Fig. 1 and Fig. 2, respectively.

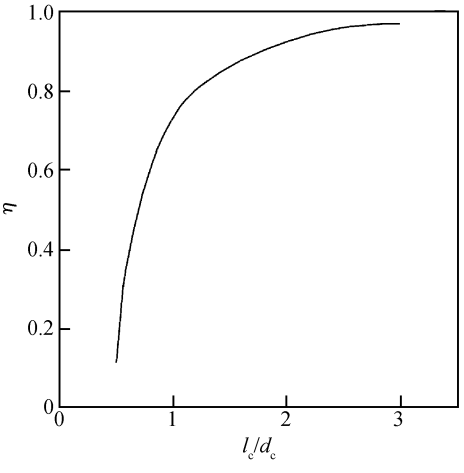

Fig. 2 Gate efficiency η versus l_c/d_c

6 Improvement on drain conductance g_d

The drain conductance, i.e.,

$$g_d = \left.\frac{\partial I_D}{\partial V_D}\right|_{V_G = \text{const}} \tag{3}$$

reflects the sensitivity of drain voltage to controlling the drain current. A large g_d indicates that a small variation in the drain voltage can give rise to a large change in the drain current. From the viewpoint of physics, the control of the drain voltage to drain current is still the modulation to the potential barrier. The drain current consists of carriers injected over a potential barrier in a depleted channel. The drain field plays an important role in reducing the barrier height and thus causing triode-like I-V characteristics. The sensitive control of the drain voltage demonstrates that the change in the potential barrier (hence the current) encounters a very small obstruction (exhibiting small drain resistance r_d), meaning high drain conductance. In order to describe the intrinsic quality of an SIT, a "sensitivity factor" of the SIT is first defined as

$$D \equiv \frac{\partial \Phi_{min}}{\partial V_D^*} \approx \frac{\mu_0}{\mu_0^2 - 1}(\mu_0^{1/2} - \mu_0^{-1/2}) \tag{4}$$

where V_D^* is the intrinsic drain voltage that is linearly proportional to V_D. The sensitivity factor D is only determined by the ratio of length to thickness of channel l_c/d_c as shown in Fig. 3.

The drain conductance depends strongly on device geometry. High drain conductance can be realized only in short channel devices (small l_c). The

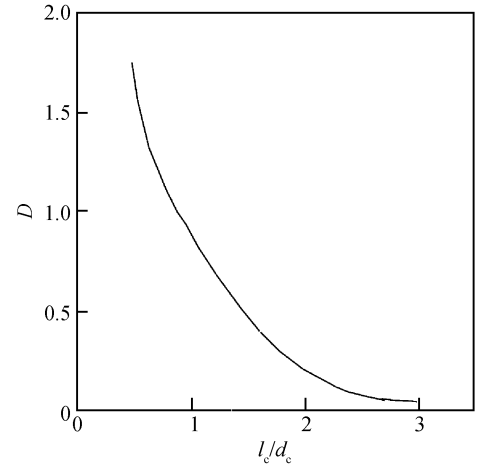

Fig. 3 Dependence of sensitivity factor D on l_c/d_c

channel thickness d_c is an essential parameter in determining drain conductance. The drain conductance is determined by the ratio l_c/d_c of channel length and thickness. In other words, the channel should be short, but rather thick (large space between the gate stripes). This requirement means that a high frequency high power SIT has to be manufactured using a shallow junction technique. Only when the channel is very short can the drain field along the channel penetrate into the depleted region that expands from the gate (perpendicular to the drain field), making the height of the potential barrier lower and even vanish. As long as this condition occurs, the drain field can directly act on the source region. Correspondingly, a vast number of carriers are injected into the channel, and triode-like *I-V* characteristics appear. With the increase in channel length, the effect of drain field on the potential barrier is significantly weakened. Therefore, a long channel will make it difficult for the carriers to be injected into the channel, for the potential barrier height to be reduced, and for the velocity at which the potential barrier disappears to be decreased or to vanish. Another way to enhance the drain current is to increase the source length. But this brings about an increase in stray capacitance. It is therefore necessary to use fine patterning to attain the high current level without increasing the capacitance.

7 Optimum criterion dimensions of the channel

The controlling sensitivity of gate voltage for the current and that of drain voltage are contradictory in requirements for dimension parameters l_c/d_c of the channel. The former requires large l_c/d_c, but the latter needs small l_c/d_c. To satisfy the two requirements simultaneously, an appropriate trade-off must be made. The minimum length of channel is chosen if possible. The experimental results demonstrate that when the value of $l_c/d_c \approx 1$, the potential barrier is in a crucial state in which the drain current can be sensitively modulated by both drain and gate voltages. In the ideal situation, if the SIT has vertical *I-V* characteristics as shown in Fig. 4, a series of parameters in the large current region will be much improved. Unfortunately, it is difficult to obtain such ideal

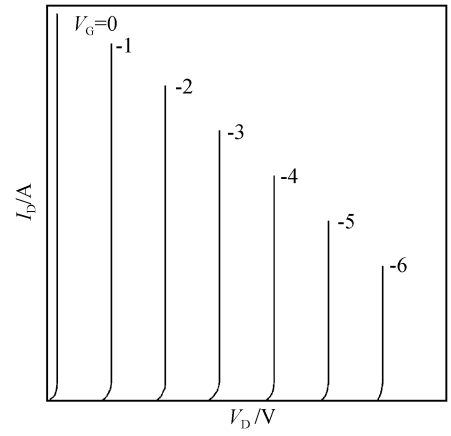

Fig. 4　Ideal *I-V* characteristics of SIT

I-V characteristics like these. But the ideal *I-V* characteristics of the SIT shown in Fig. 4 can be used to help us to understand the meanings of D and η as well as large current performance.

8 Influence of voltage amplification on current performance

According to the relation $g_m = \mu g_d$, it is important for us to increase voltage amplification μ, so as to improve the large current characteristics. The voltage amplification factor μ may be represented as

$$\mu = \frac{1}{\alpha_D}\mu^* = \frac{\mu_0 + 1 - 2\sqrt{\mu_0}}{\alpha_D \sqrt{\mu_0}} \tag{8}$$

where $\alpha_D = 0.2$. The experimental relationship between μ and l_c/d_c is given in Table 3.

Obviously, with the increase of the ratio l_c/d_c, the "voltage amplification factor" μ, "gate efficiency" η, and "trans-conductance" g_m, will be increased, but the "sensitivity factor" D will be reduced. Therefore, some trade-offs must be made among these parameters. For a given d_c, the larger the length of channel l_c is, the higher the voltage amplification factor μ will be. However, the length of channel l_c is limited by the requirement of the "sensitivity factor" D. The optimum matching relationship must be considered among μ, g_m and g_d.

Table 3　Voltage amplification μ versus l_c/d_c relationship

l_c/d_c	0.5	1.0	1.5	2.0	2.5	3.0
μ	3.3	15.1	43.3	105.9	243.9	546.6

To satisfy the requirements for raising g_m, the thickness of channel d_c must be reduced, which is coincident with that for improving μ and the breakdown voltage BV_{GDO}, but contradictory to the improvement of g_d, indicating that a large current and high voltage cannot be achieved simultaneously. Some technological approaches are developed for resolving this problem, as follows:

(1) To increase the thickness of epitaxial layer properly;

(2) To reduce the doping concentration of epitaxial layer appropriately;

(3) To use the passivation process;

(4) To etch a trench between the source and gate regions;

(5) To decrease the doping concentration of the source and gate regions;

(6) To remove BSG and PSG;

(7) To increase the thickness of the second epitaxial layer;

(8) To lessen the density of diffused phosphor.

9 Impact of packaging processes on high current performance

The packaging processes also have an important impact on the high frequency current characteristics of SITs. In order to achieve excellent electrical performance, the following packing technological measures have been adopted in our experiments:

(1) The appropriate packaging case must be used to satisfy the requirements, such as small heat resistance or quick heat emission, very small parasitical parameters and reliable insulation between electrodes and packaging case.

(2) In order to reduce the lead inductances, especially L_s, the number of lead lines should be increased, but the length of each lead must be as short as possible, and parallel leading wires must be arranged reasonably.

(3) The increase of resistances R_s, R_g, and R_d that resulted from the packaging process has to be eliminated carefully; the thickness of the silicon wafer must be diminished. Au-Sb alloy should be used in sintering, and Al-Mo-Pt electrodes on the front are sintered in H_2 atmosphere.

(4) For a high frequency SIT of 2GHz, the internal matching lead inductance and MOS capacitance are also required.

10 Results and conclusions

It has been experimentally and theoretically demonstrated that an SIT consisting of many parallel units with a great number of channels has combinational comprehensive electrical performances. The total g_m of an SIT is obviously increased if many units are connected in parallel, even larger than the sum of their respective single value. The methods to increase the output current are to enhance the capability of the output current and the sensitivity of the controlling current, which are characterized by the parameters of trans-conductance g_m and drain conductance g_d. Therefore, it is suggested that in order to improve the high current performance of an SIT, a structure of multiple units in parallel with a large number of channels should be used. The significant factors first defined in this paper, including transconductance per unit channel width, gate efficiency, the sensitivity factor and intrinsic static gain, that can be used to describe the electrical performance from different viewpoints in the research and production of SITs.

When speaking of electrical performance of SITs in this paper, it is the completely packaged device (not the unpackaged chip) that exhibits these characteristics. It is impossible to obtain high performance only from perfect structure designs and advanced fabrication technologies. It should be pointed out that excellent performance can never be realized by an unskilled packaging technology and an inferior packaging case. The structure design, the fabrication technology and packaging technique are all important for acquiring high performance; they must be matched optimally.

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静电感应晶体管大电流特性的改善

王永顺†　吴　蓉　刘春娟　李思渊

（兰州交通大学电子与信息工程学院，兰州　730070）

摘要：描述了改善静电感应晶体管(SIT)大电流特性的新方法.首次定义了从不同角度表征 SIT 电特性的重要因子,如单位沟道宽度跨导、栅效率、灵敏度因子和本征静电增益.从理论和工艺实践上研究了这些因子与几何结构之间的关系,揭示了器件电性能对几何结构和工艺参数的依赖关系.设计建立了 SIT 频率参数和功率参数测试方法和电路,深入讨论了封装工艺对 SIT 电性能的影响.

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† 通信作者.Email:wangysh@mail.lzjtu.cn
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